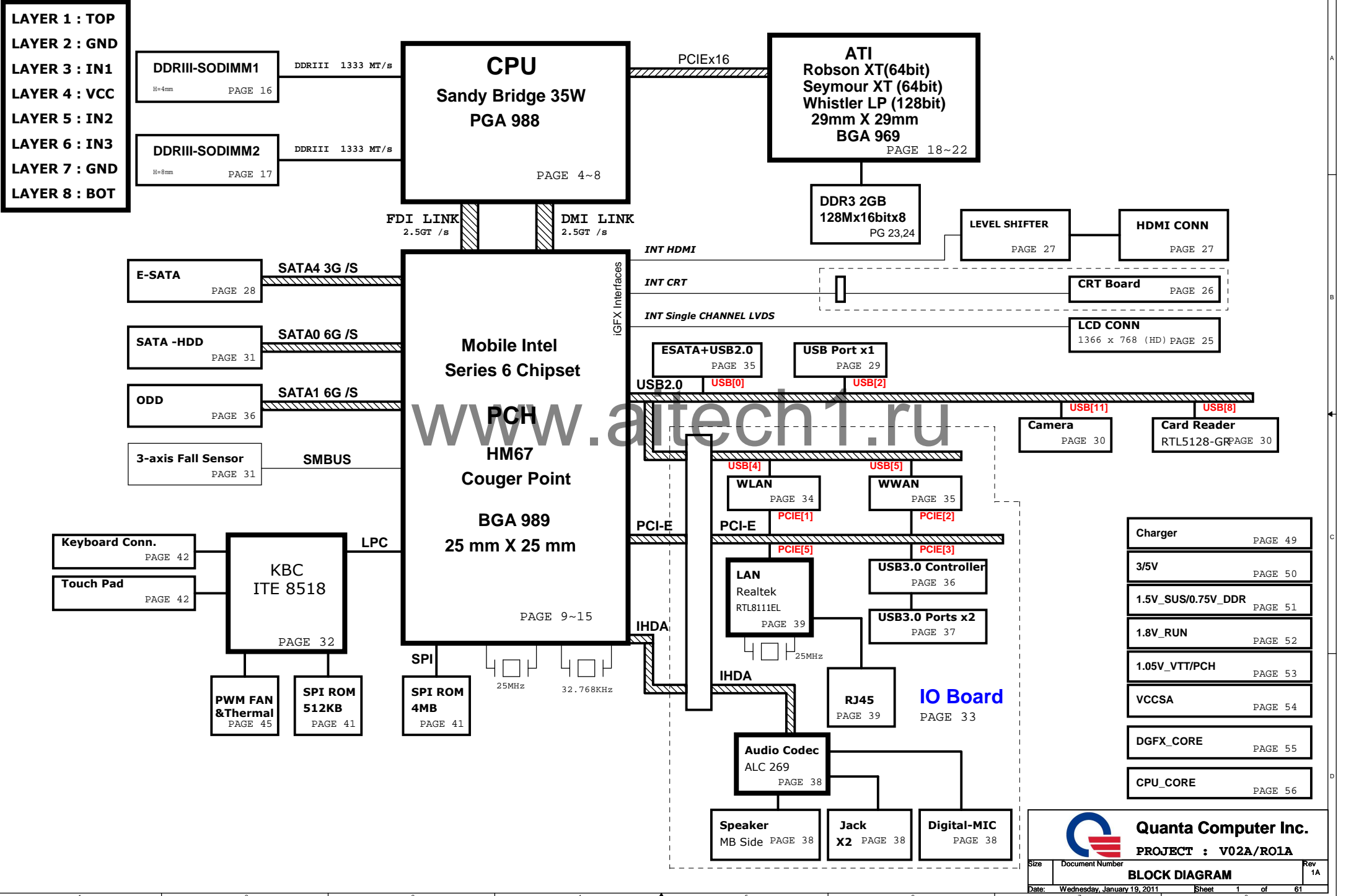


# V02A/R01A DIS BLOCK DIAGRAM





power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

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SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								



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**PROJECT : V02A/R01A**

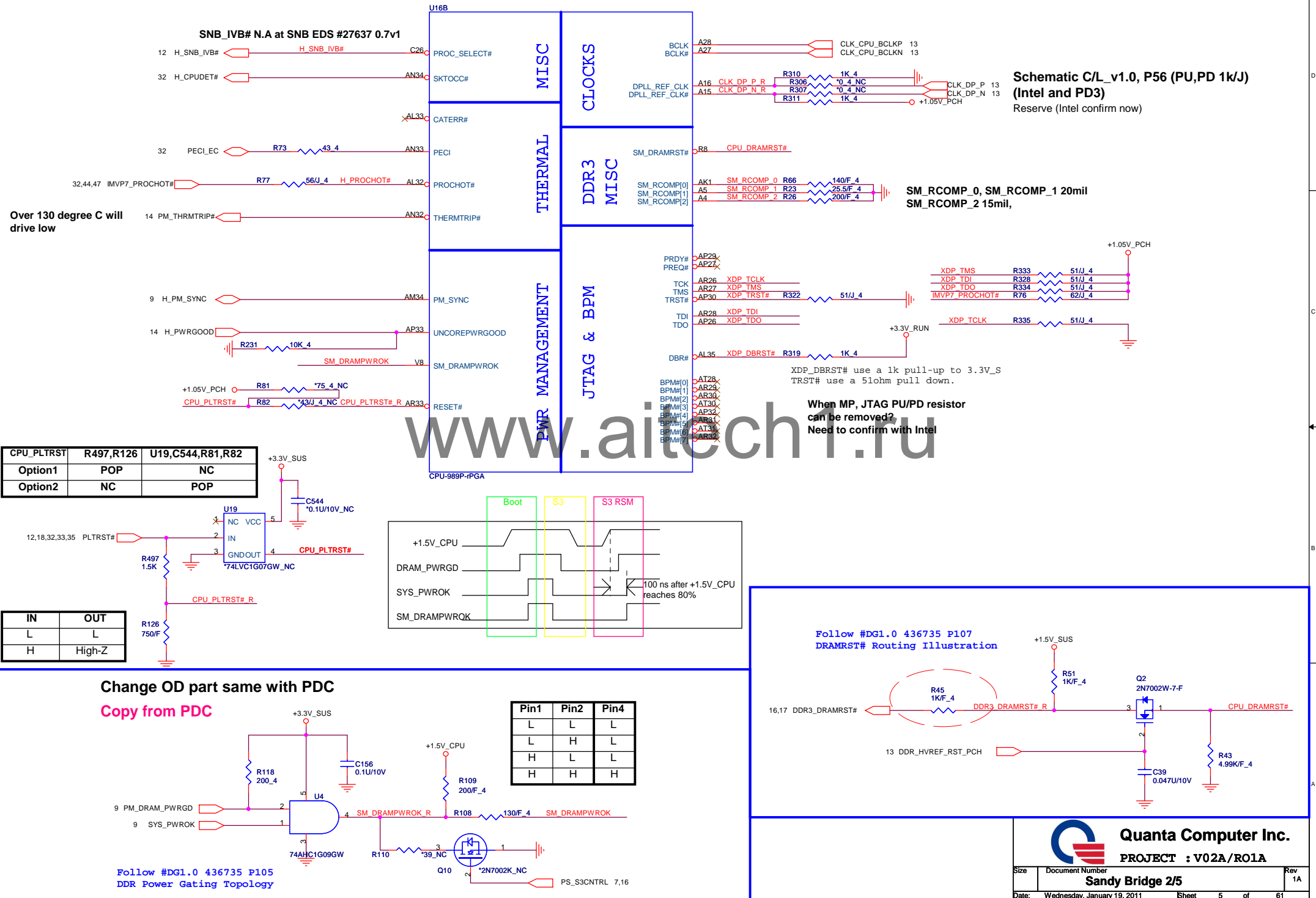
Size	Document Number	Rev
	<b>BLANK</b>	<b>1A</b>
Date:	Wednesday, January 19, 2011	Sheet 3 of 61





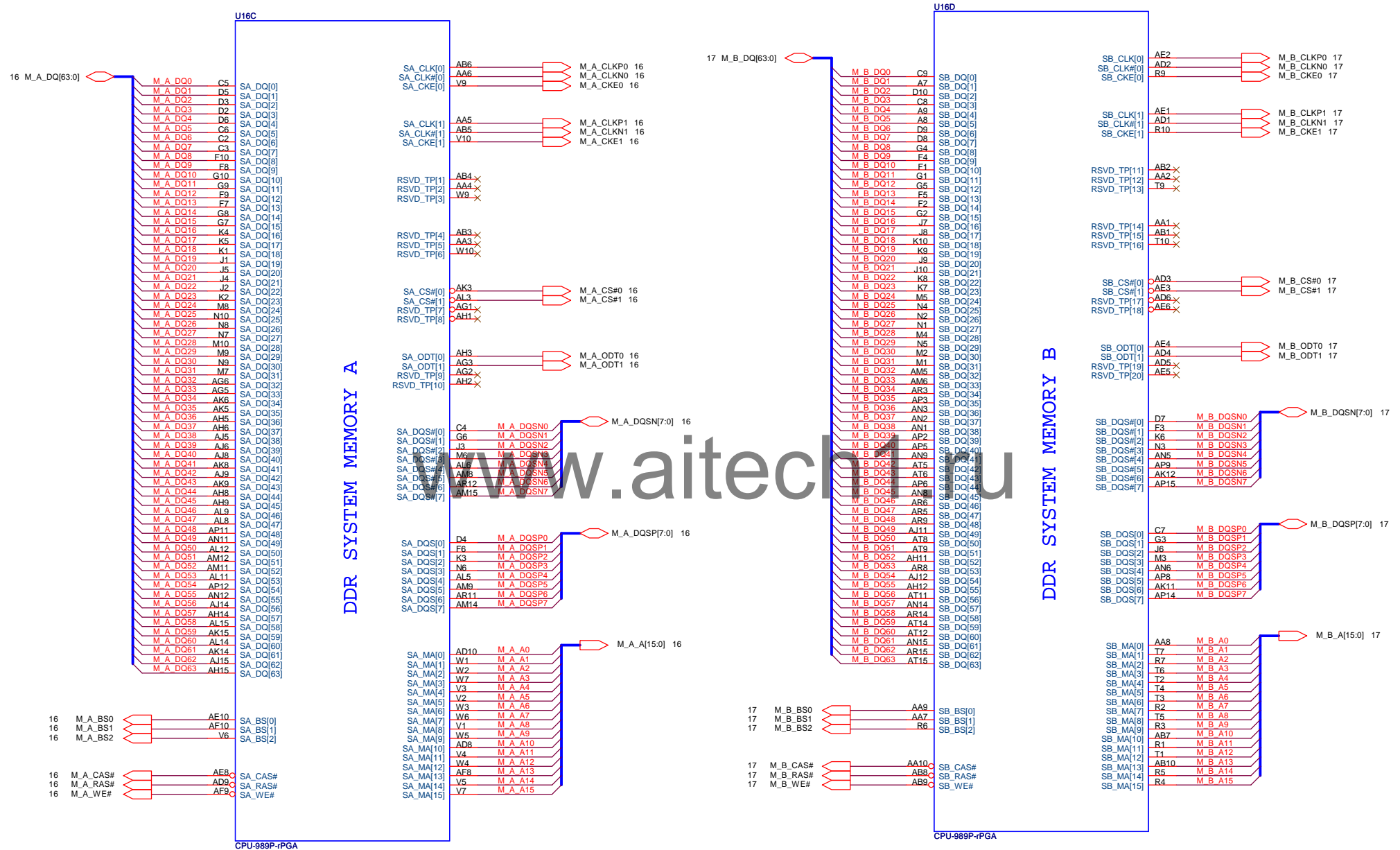


# Sandy Bridge Processor (CLK,MISC,JTAG)





## Sandy Bridge Processor (DDR3)





## Sandy Bridge Processor (POWER)

CPU VTT  
SNB 35W:8.5A  
10F x12CPU VGT  
SNB 35W:22A  
10uF x 12

## Sandy Bridge Processor (GRAPHIC POWER)

## POWER

## GRAPHICS

## 1.8V RAIL

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

## SENSE LINES

## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

## SENSE LINES

## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

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## SA RAIL

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## SA RAIL

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## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

## SENSE LINES

## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

## SENSE LINES

## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

## MISC

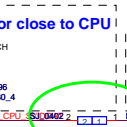
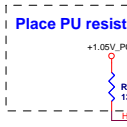
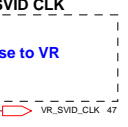
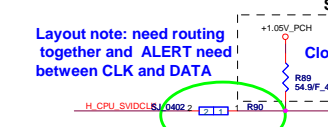
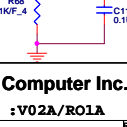
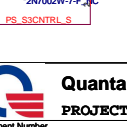
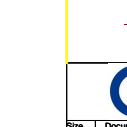
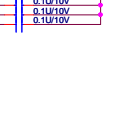
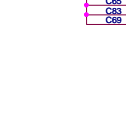
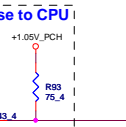
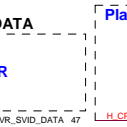
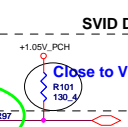
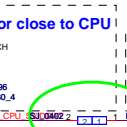
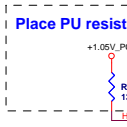
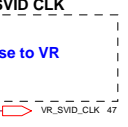
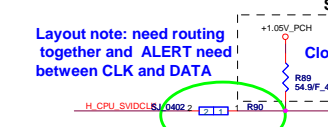
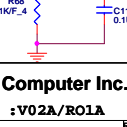
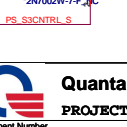
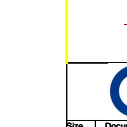
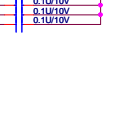
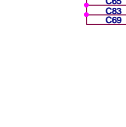
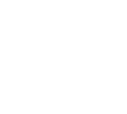
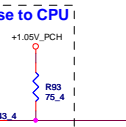
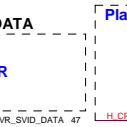
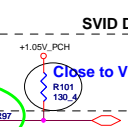
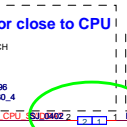
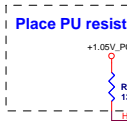
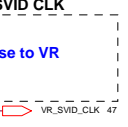
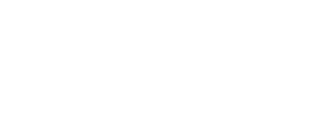
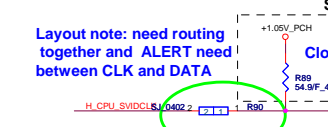
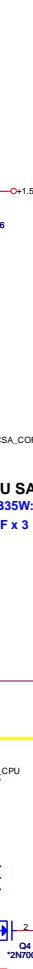
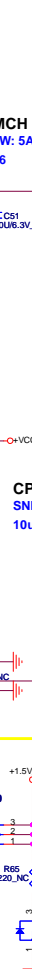
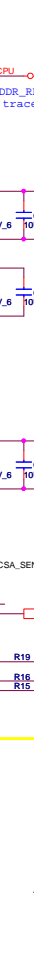
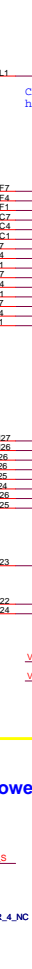
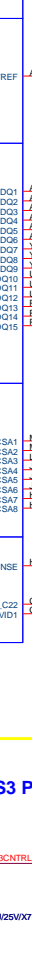
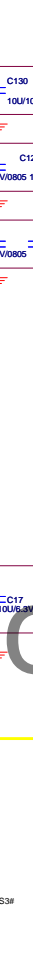
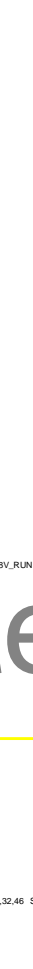
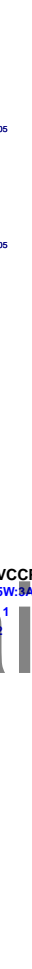
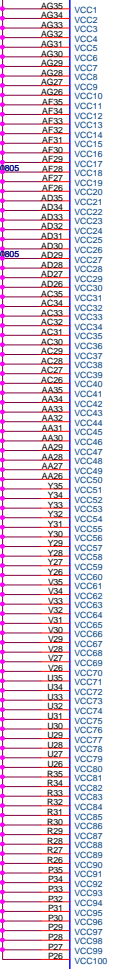
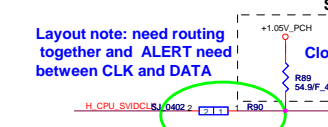
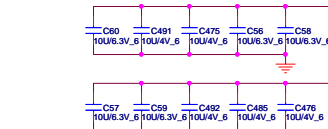
## SENSE LINES

## VREF

## DDR3 - 1.5V RAILS

## SA RAIL

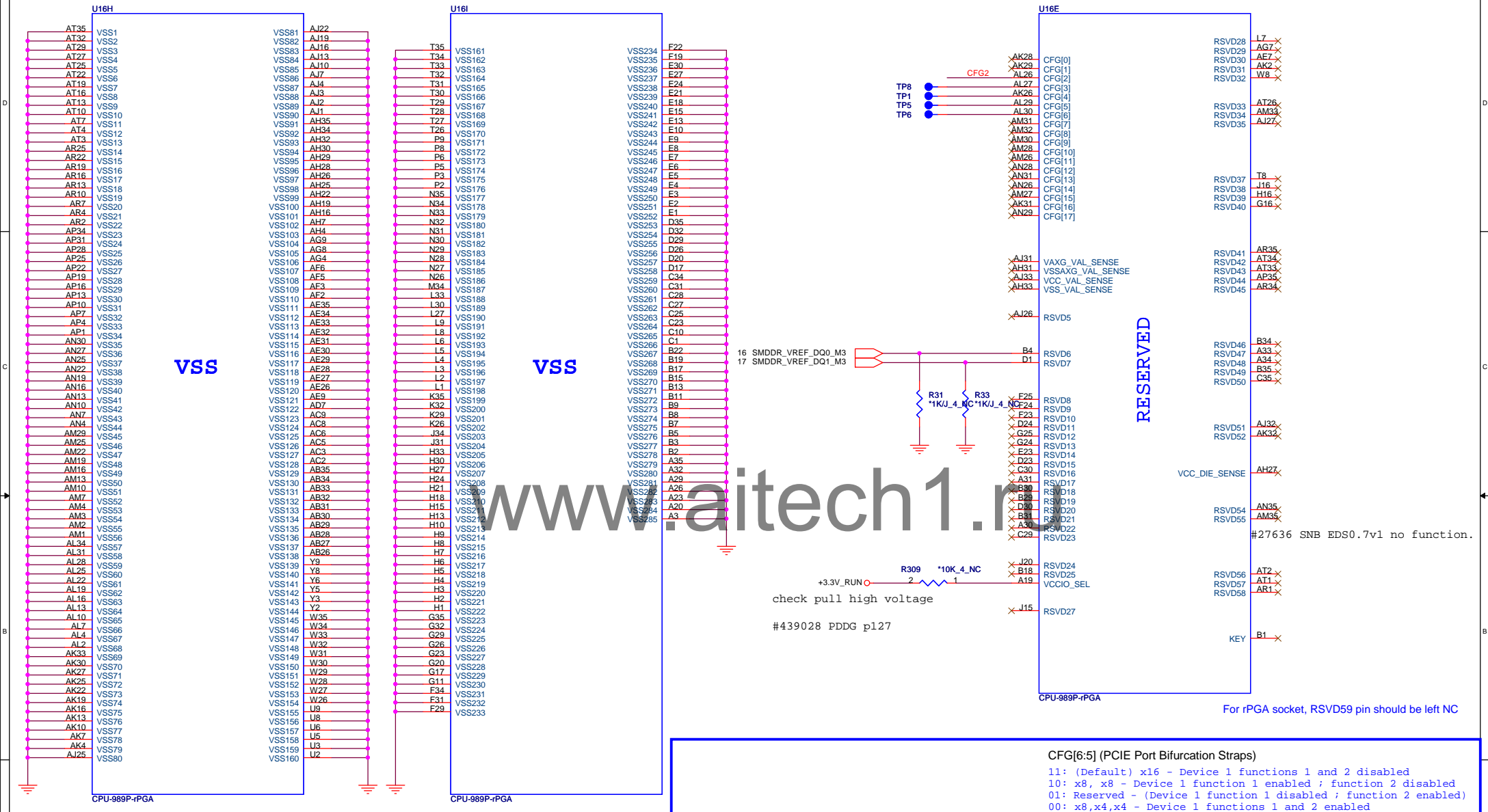
## MISC

CPU Core Power  
SNB 35W:55A  
10uF x 24



## Sandy Bridge Processor (GND)

## Sandy Bridge Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R106 1K/4

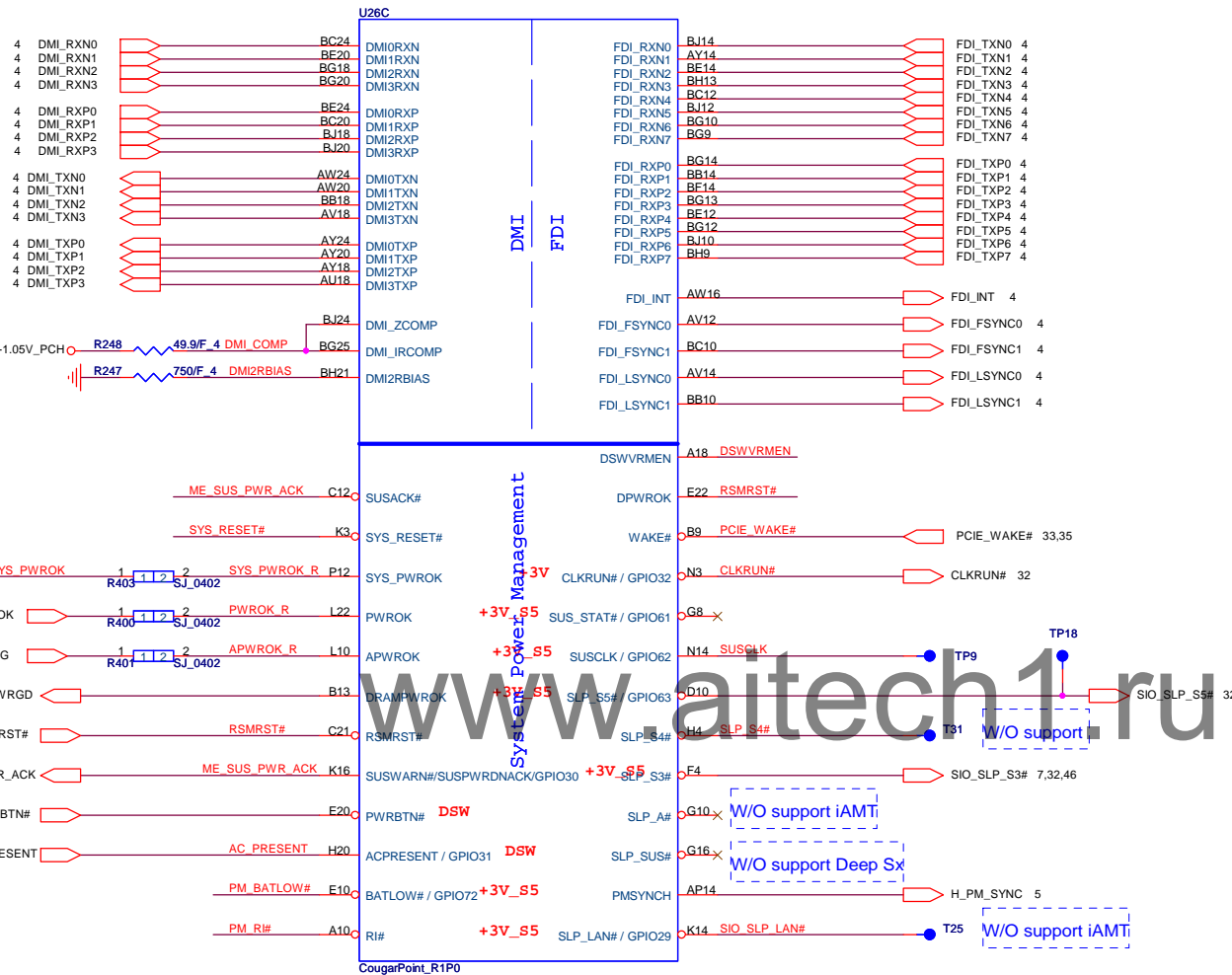


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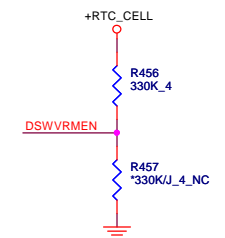
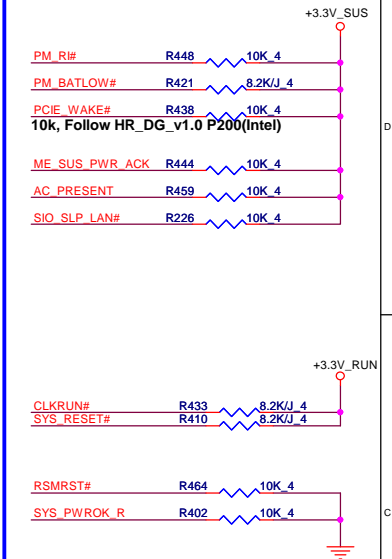
PROJECT : V02A/RO1A



Cougar Point (DMI,FDI,PM)

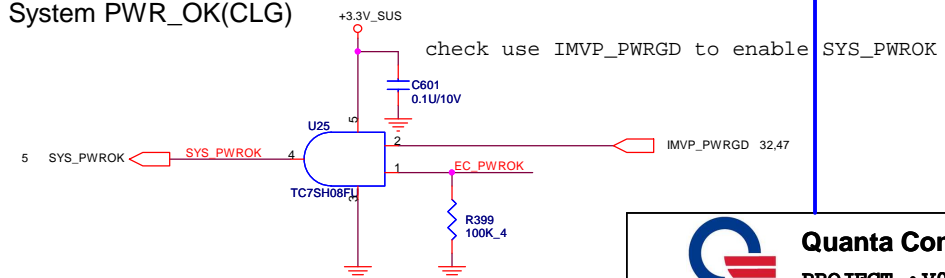


PCH Pull-high/low(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

## System PWR\_OK(CLG)



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**PROJECT : V02A/R01A**

PROJECT : V02A/R01A

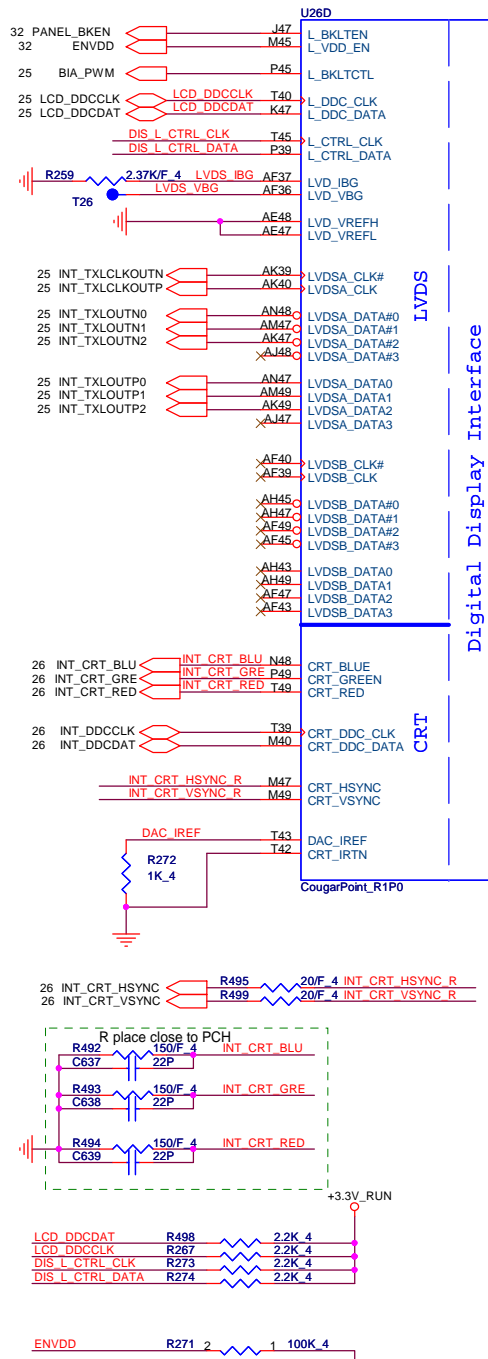
**Cougar Point 1/7**

Date: Wednesday, January 19, 2011 Sheet 9 of 61

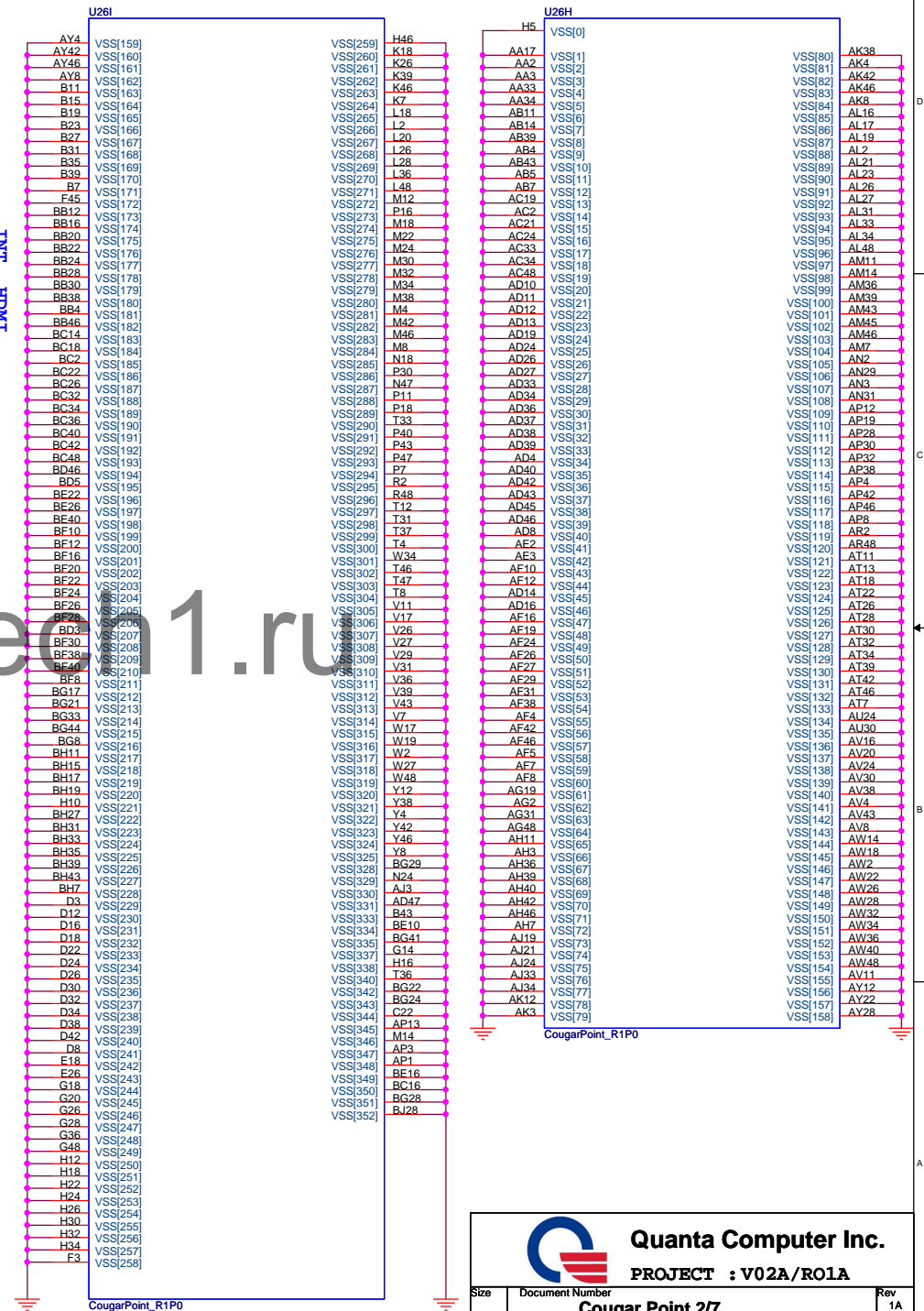
Date: Wednesday, January 19, 2011 Sheet 9 of 61



## Cougar Point (LVDS,DDI)

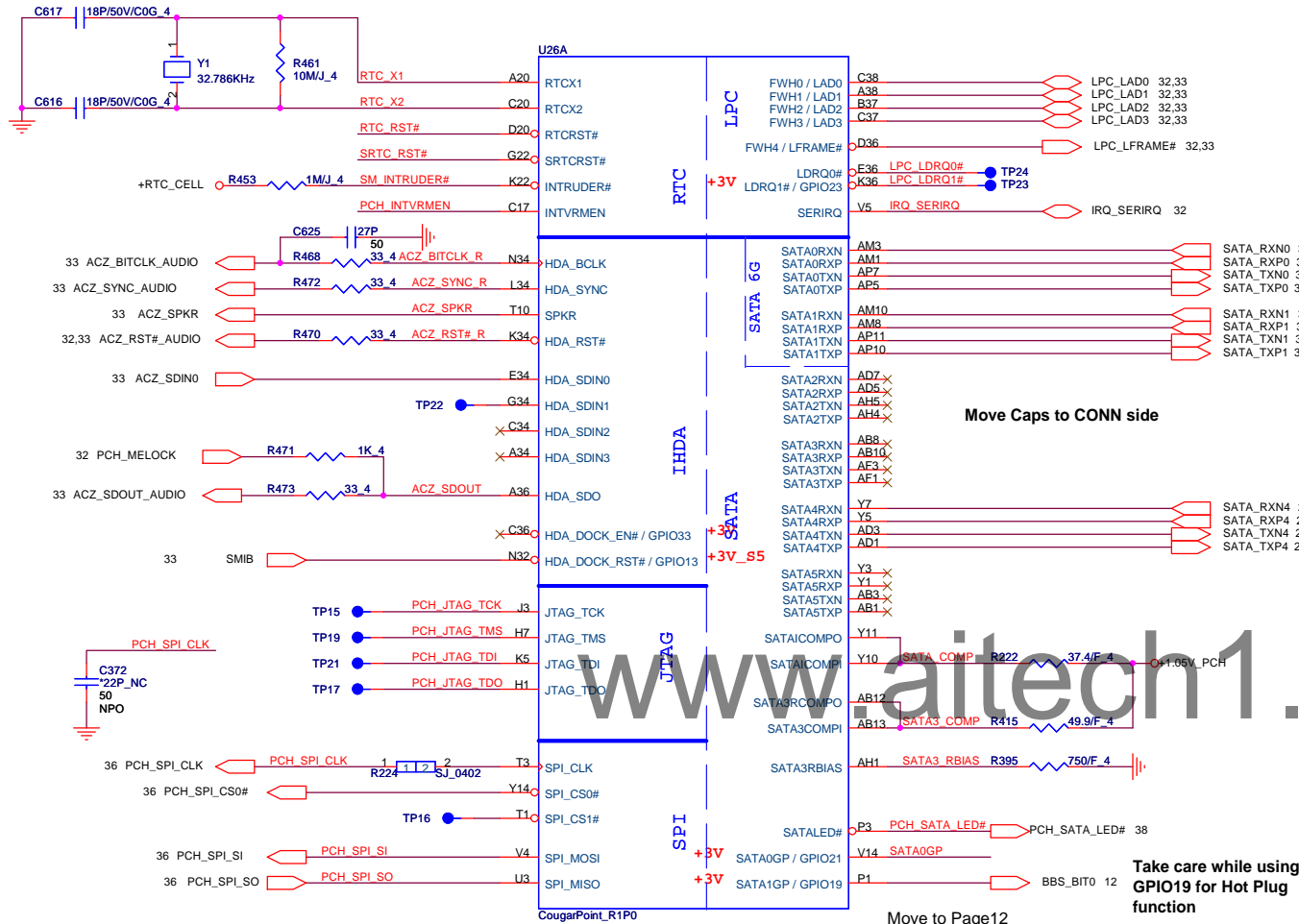


Cougar Point (GND)



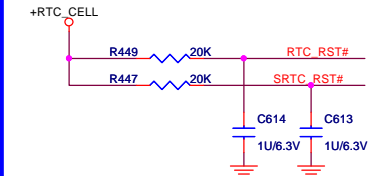
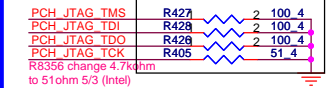
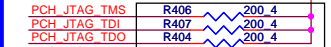


# Cougar Point (HDA,JTAG,SATA)



## PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



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Move to Page12

Take care while using GPIO19 for Hot Plug function

## PCH Strap Table

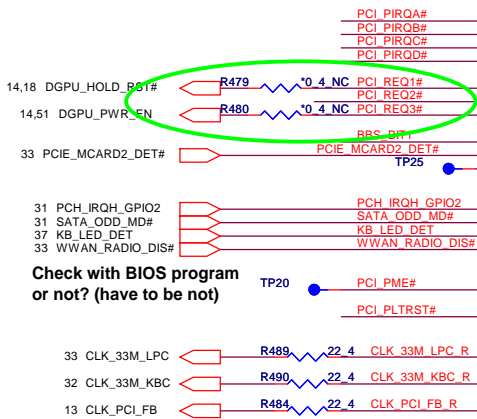
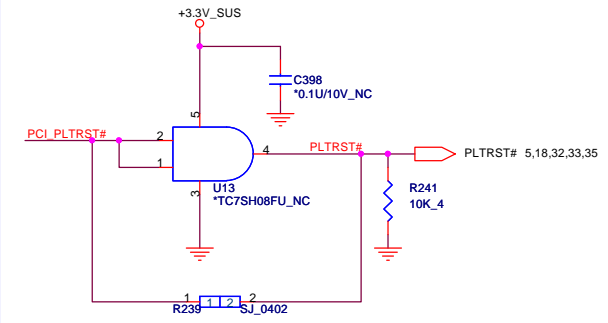
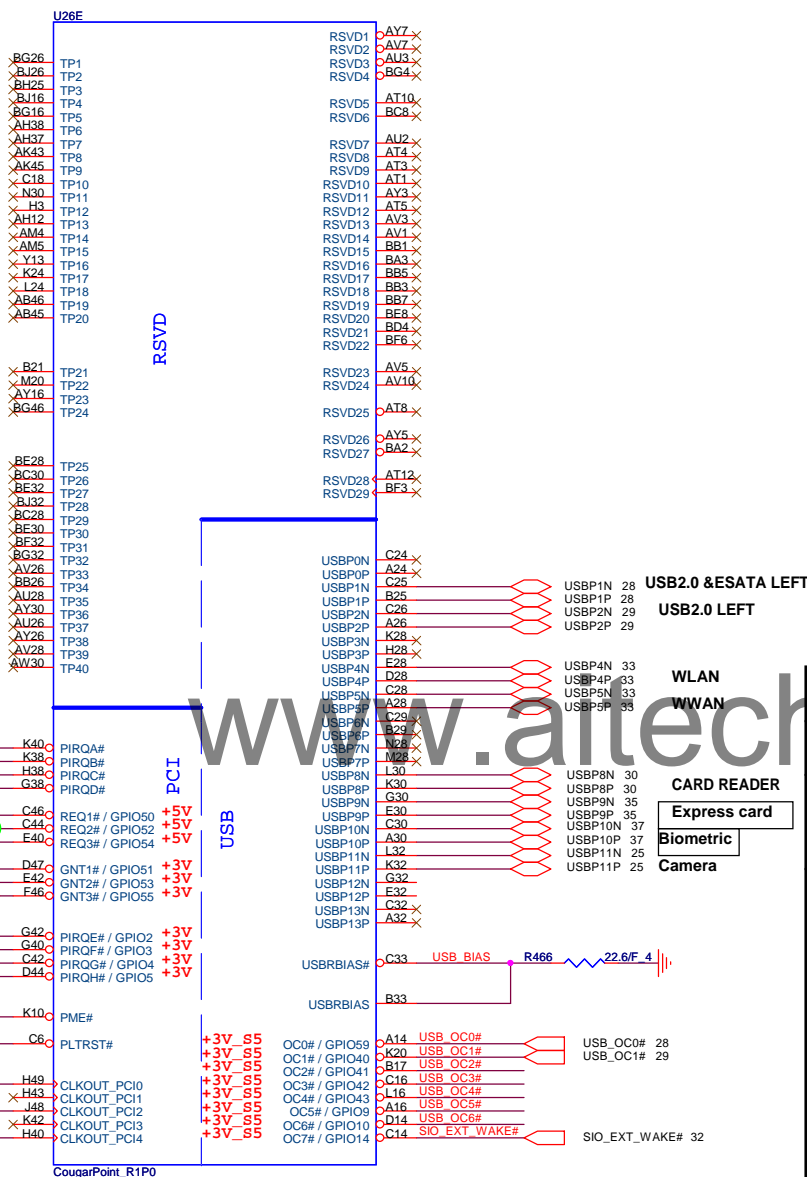
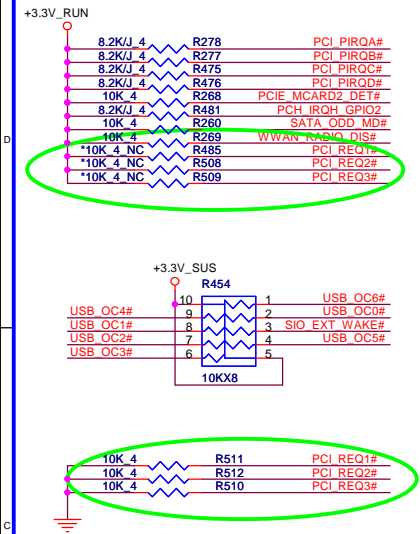
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS  R413  *1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS  R474  *1K 4 NC ACZ_SDO
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL  R455  330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS  R469  1K 4 ACZ_SYNC_R



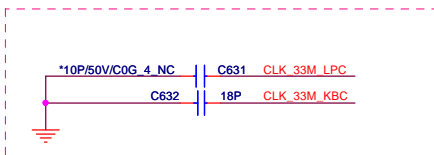
## PCI/USBOC# Pull-up(CLG)

## Cougar Point-M (PCI,USB,NVRAM)

## PLTRST#(CLG)



Check CLKOUT if Skew requirement?



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
<div><div><div>BBS_BIT1</div><div>R496</div><div>*1K 4_NC</div></div><div>11 BBS_BIT0</div><div><div>R394</div><div>*1K 4_NC</div></div><div></div></div> <div>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</div>												
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
<div><div><div><div>R420</div><div>2.2K 4</div><div>+1.8V_RUN</div></div><div><div>R424</div><div>2</div><div>1</div><div>SJ_0402</div></div><div>DF_TV5 14</div><div>H_SNB_IVB# 5</div></div><div>CheckList_1.0 p58; HR_v1.0 p450</div></div>												



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PROJECT : V02A/RO1A



## U26B



CLK_DMIN	R244	10K 4
CLK_DMIP	R245	10K 4
CLK_BUF_DREFCLKN	R465	10K 4
CLK_BUF_DREFCLKP	R467	10K 4
CLK_BUF_DREFSSCLKN	R206	10K 4
CLK_BUF_DREFSSCLKP	R205	10K 4
CLK_PCH_14M	R488	10K 4

		<b>Quanta Computer Inc.</b> <b>PROJECT : V02A/RO1A</b>	
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<b>Cougar Point 5/7</b>			
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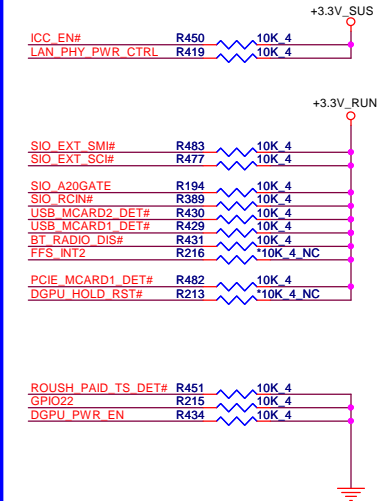


## Cougar Point (GPIO,VSS\_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



### GPIO Pull-up/Pull-down(CLG)



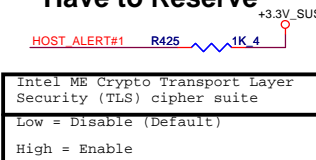
Add Description  
in EC GPIO table  
(keyboard  
controller reset)

Check When Symbol Update (OK)

### Can be del



### Have to Reserve



### MFG-TEST



**Quanta Computer Inc.**  
**PROJECT : V02A/RO1A**

Size	Document Number	Rev
	<b>Cougar Point 6/7</b>	1A
Date	Wednesday, January 19, 2011	Sheet 14 of 61

DO NOT program this pin (BIOS)



### SGPIO Confirm with Intel



BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is  
for intel BIOS validation purpose.

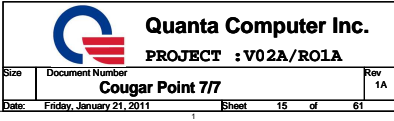
BMBUSY#:  
If not used, require a weak pull-up  
(8.2- KΩ to 10 KΩ) to Vcc3\_3.  
CRB(V1.0)P28: it has 1K PU and  
100 ohm on this net for validation purpose.

DMI TERMINATION  
VOLTAGE OVERRIDE

Low = Tx, Rx terminated to  
same voltage (DC Coupling Mode)  
(DEFAULT)

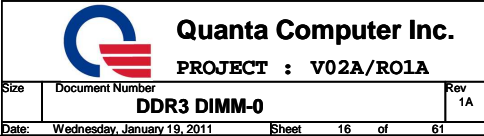


Cougar Point (POWER)



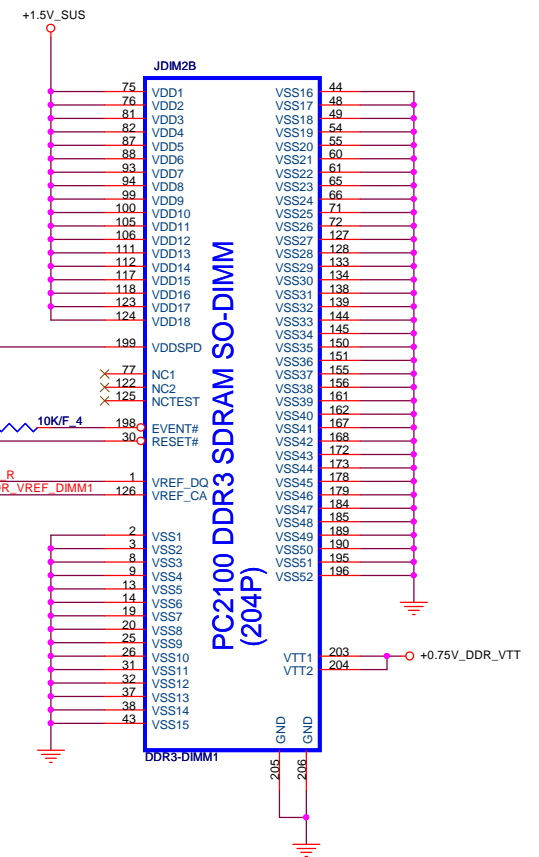
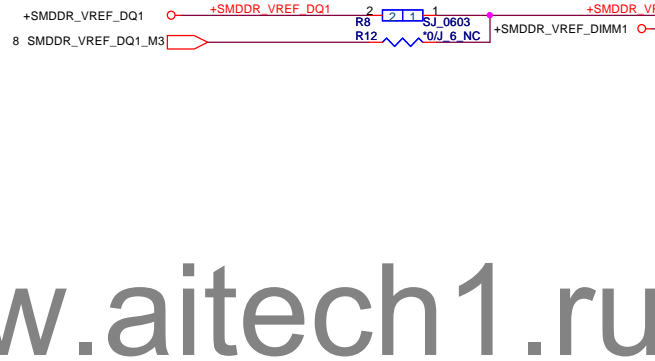
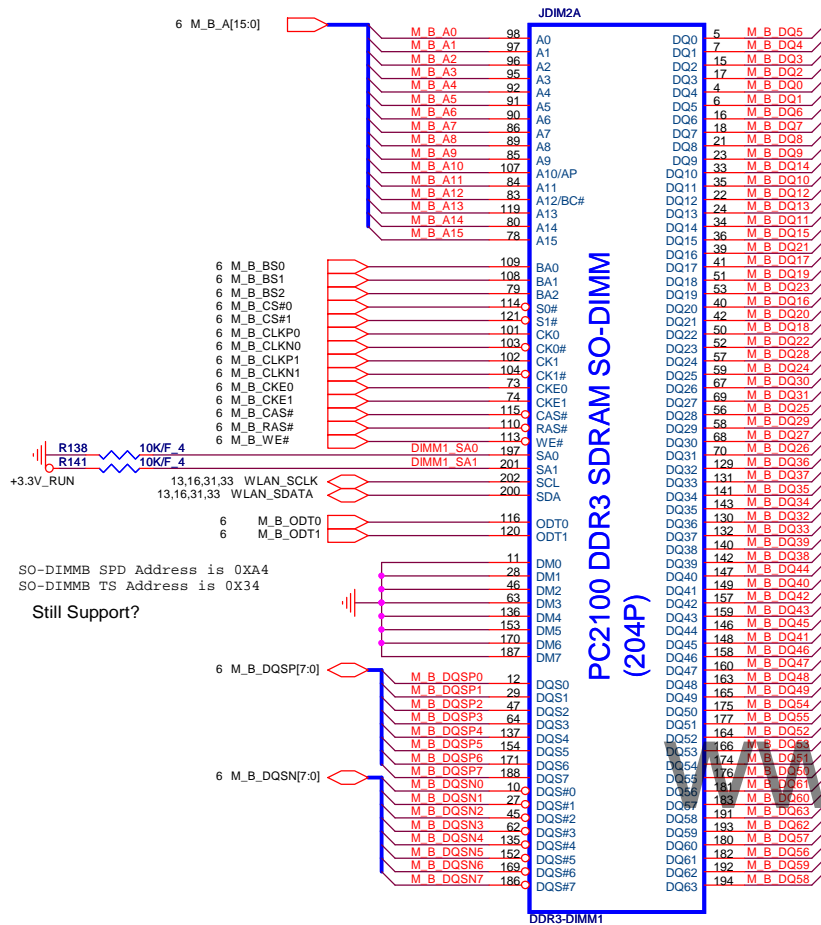


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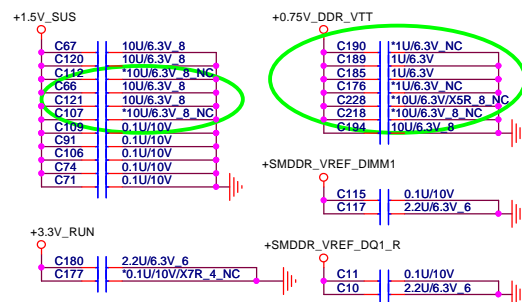


H=4mm,RVS

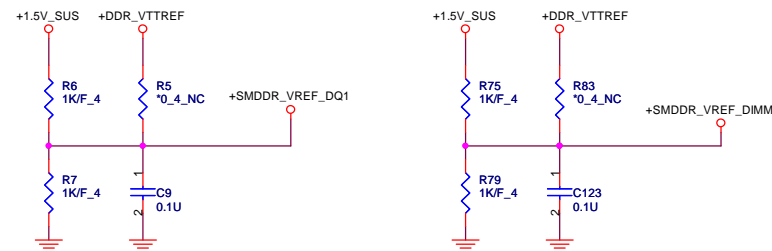


### Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%



### M1 VREF



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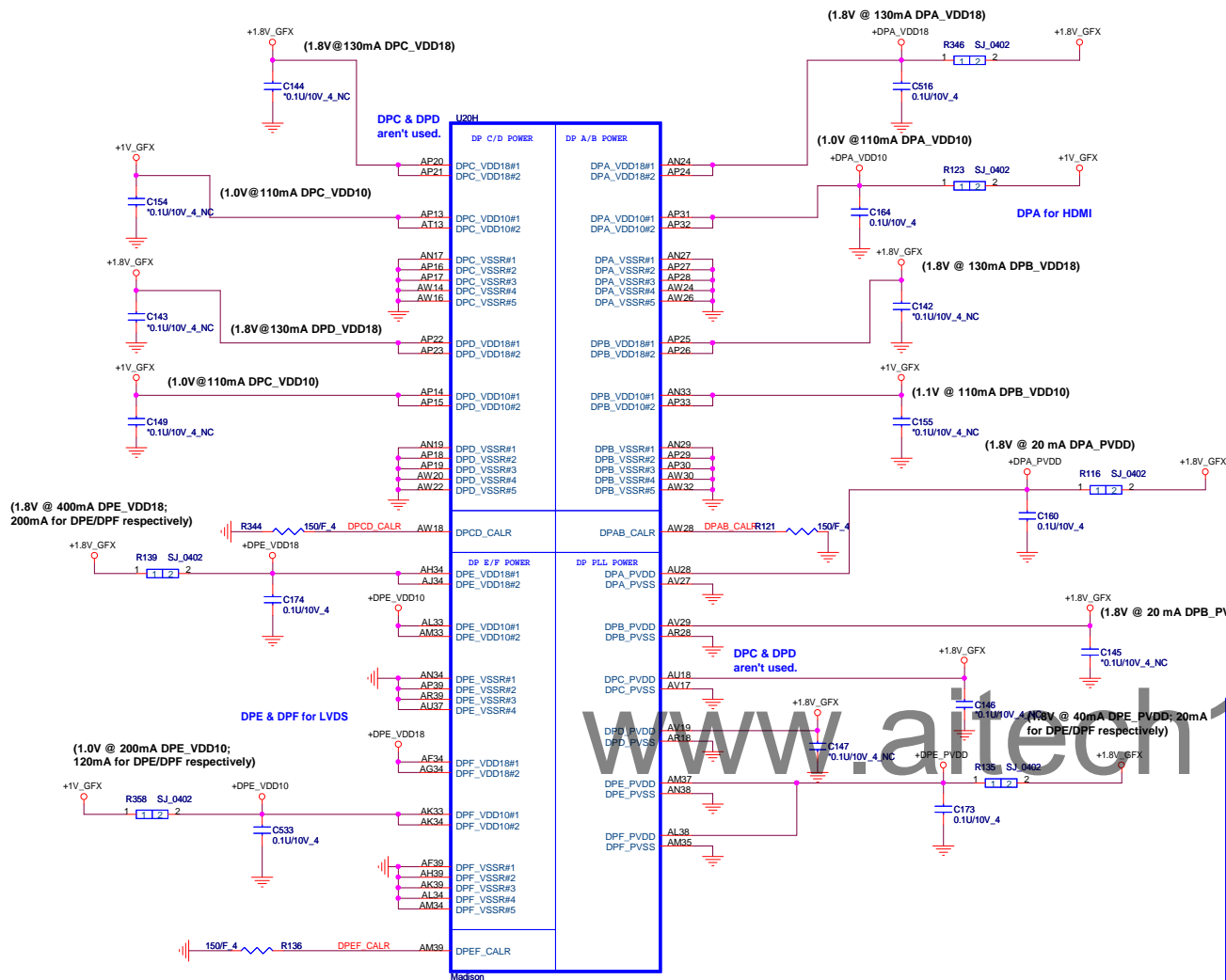












- ### GPU Power Rail List
- |            |             |
|------------|-------------|
| +1V_GFX=>  | +1.8V_GPU=> |
| +DPA_VDD10 | +A2VDDQ     |
| +SPV10     | +AVDD       |
| +DPE_VDD10 | +DPA_PVDD   |
| +DPLL_VDDC | +DPA_VDD18  |
| +PCIE_VDDC | +DPE_PVDD   |
|            | +DPE_VDD18  |
|            | +DPLL_PVDD  |
|            | +MPV18      |
|            | +PCIE_PVDD  |
|            | +PCIE_VDDR  |
|            | +SPV18      |
|            | +TSVDD      |
|            | +VDD1DI     |
|            | +VDD2DI     |
|            | +VDD_CT     |
|            | +VDDR4      |

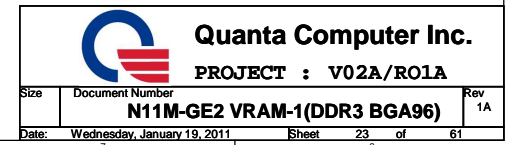
- ### GPU Power-on sequence
- 1 => +3V\_GFX
  - 2 => +VCC\_DGFX\_CORE
  - 3 => +1V\_GFX
  - 4 => +1.5V\_GFX
  - 5 => +1.8V\_GFX
  - 6 => dGPU\_PWROK



20 VMA\_DQ[63..0]  
20 VMA\_DM[7..0]  
20 VMA\_WDQS[7..0]  
20 VMA\_RDQS[7..0]



VMA\_CLKP0 R391 56J\_4  
VMA\_CLKN0 R390 56J\_4  
C595 0.01U/25V\_4  
VMA\_CLKP1 R209 56J\_4  
VMA\_CLKN1 R210 56J\_4  
C356 0.01U/25V\_4





```

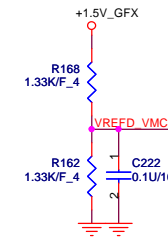
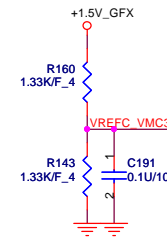
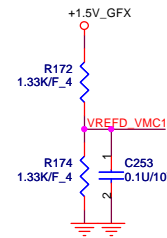
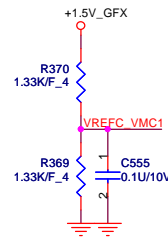
20 VMC_DQ[63..0]
20 VMC_DM[7..0]
20 VMC_WDQS[7..0]
20 VMC_RDQS[7..0]

```

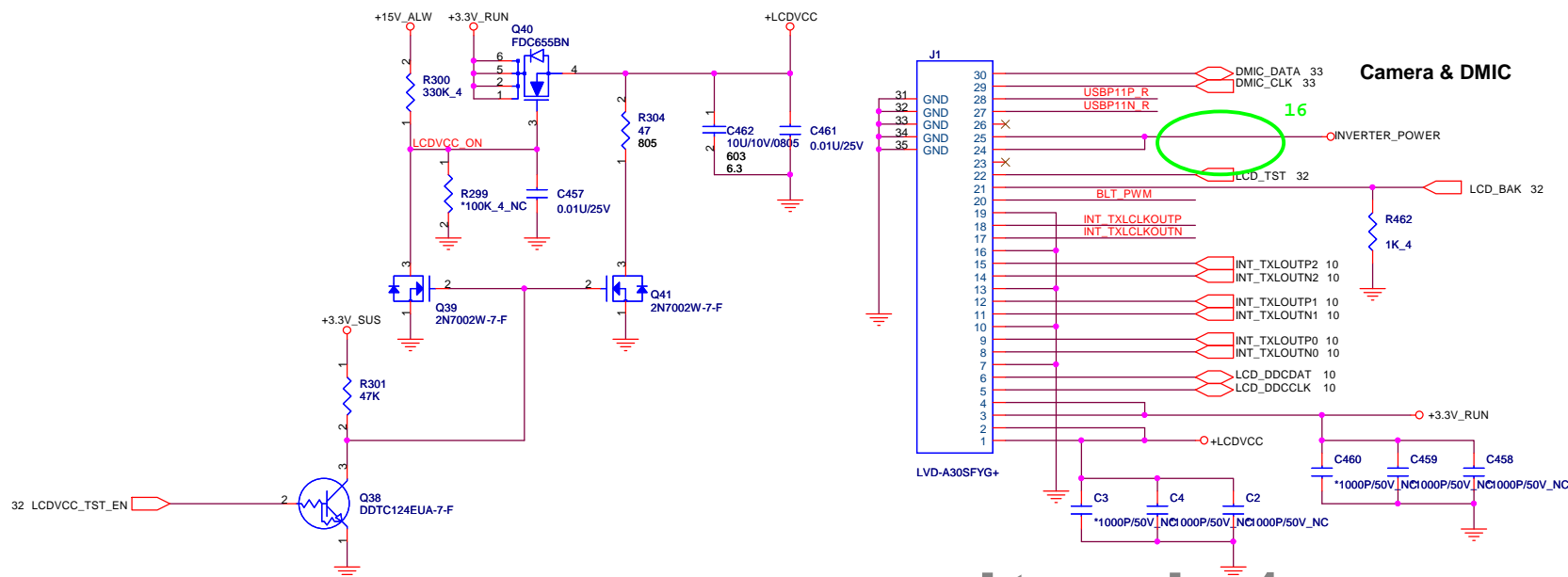


VMC\_CLKP0 R372 56/J\_4  
VMC\_CLKN0 R371 56/J\_4  
VMC\_CLKP1 R357 56/J\_4  
VMC\_CLKN1 R359 56/J\_4

C561 0.01U/25V\_4  
C530 0.01U/25V\_4

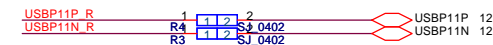
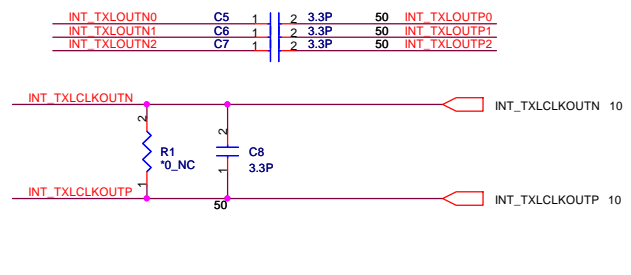
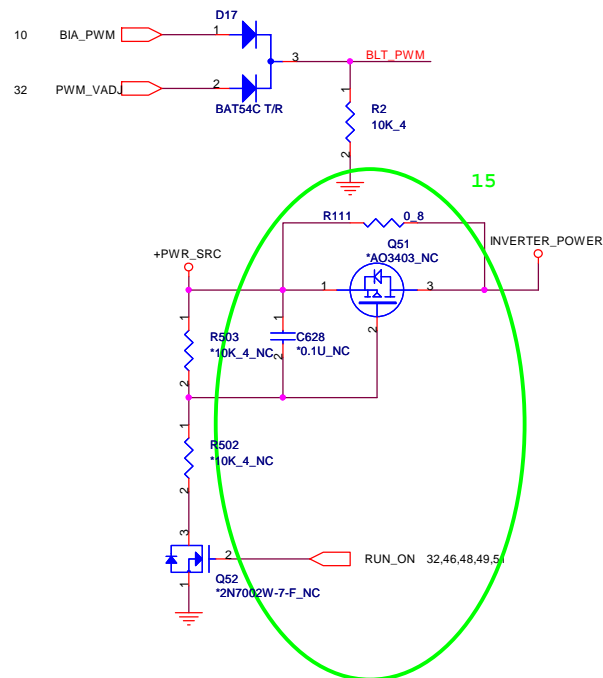






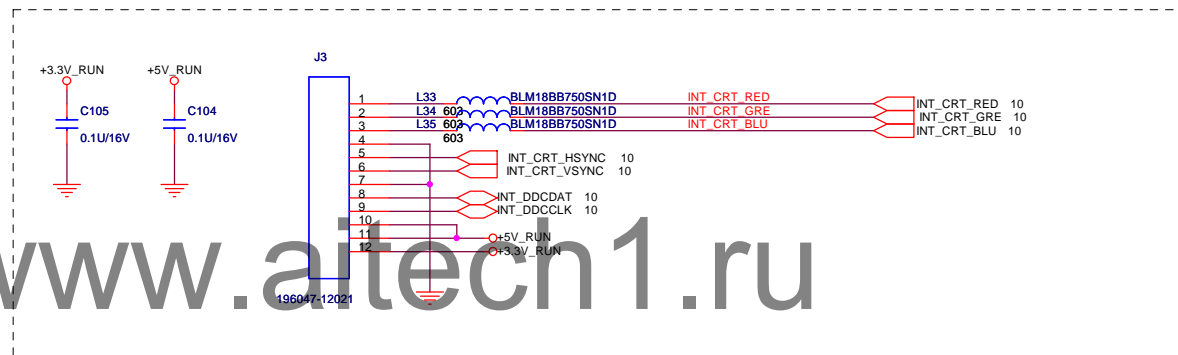
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Shunt capacitors on LVDS for improving WWAN.



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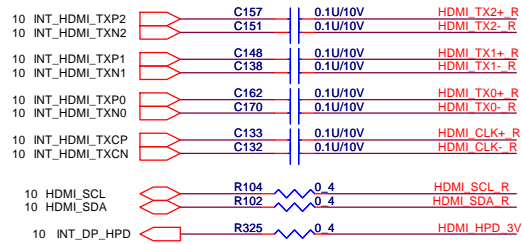
**Quanta Computer Inc.**

**PROJECT : V02A/RO1A**

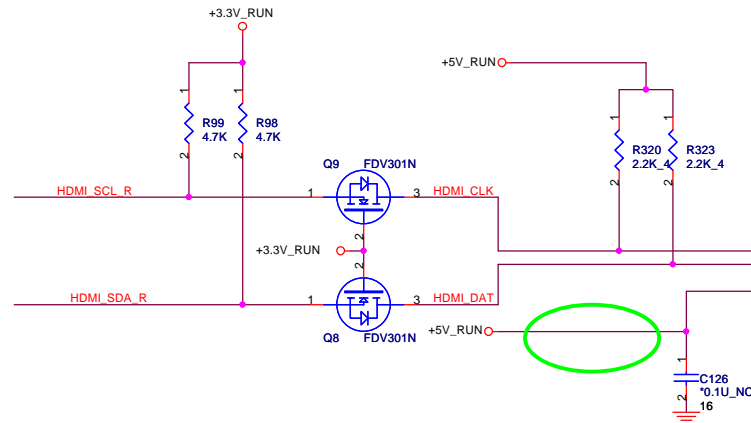
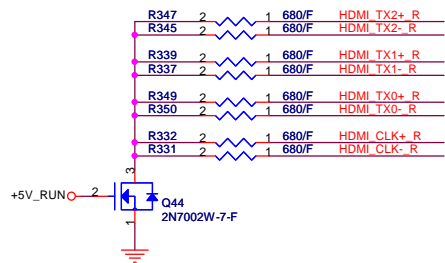
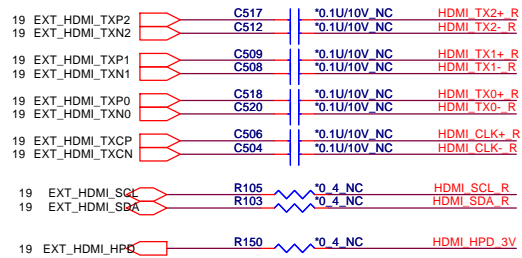
Size	Document Number	Rev
	<b>BLANK</b>	1A
Date:	Wednesday, January 19, 2011	Sheet 26 of 61



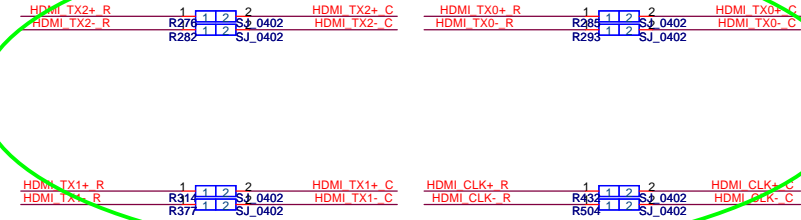
## UMA HDMI



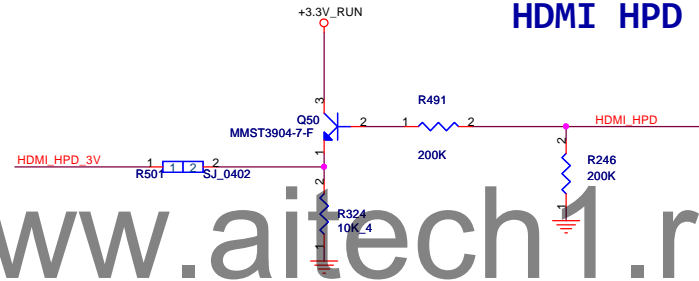
## DIS HDMI



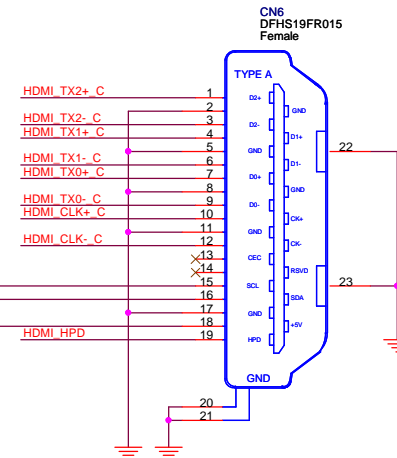
Reserve for EMI and close to HDMI CONN



## HDMI HPD



## HDMI Conn.

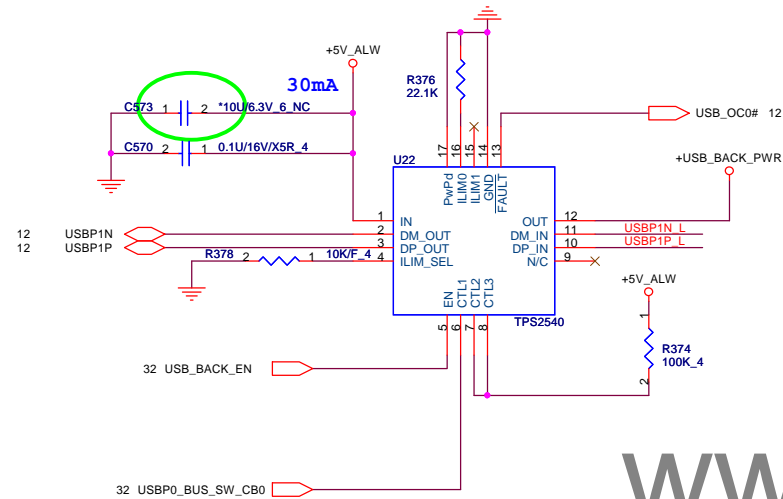


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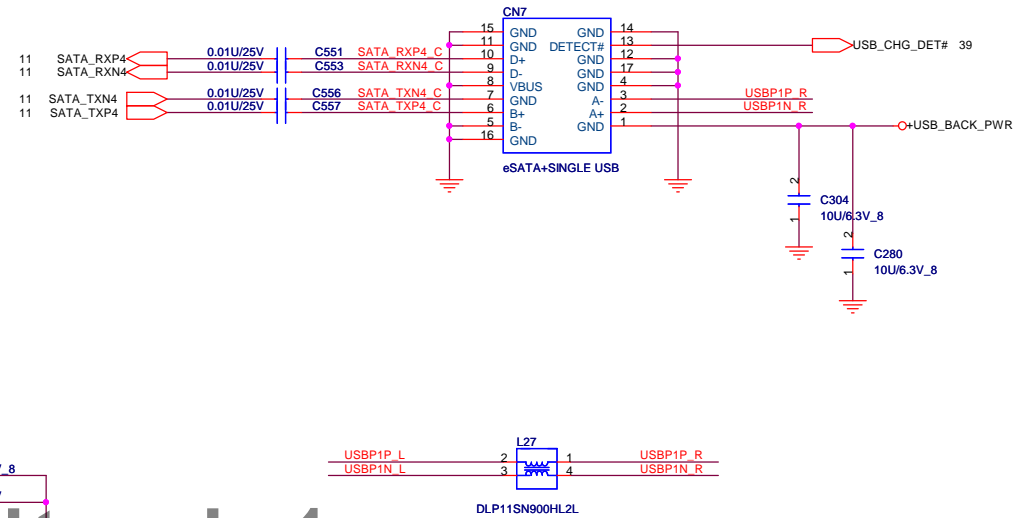
# ESATA + USB Conn + Power share

## S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

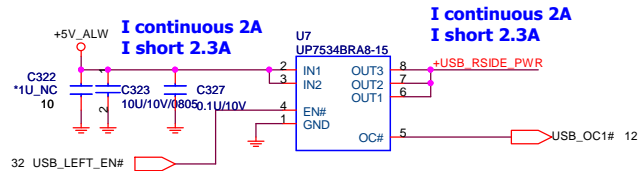
	R8224	mA	
OC	100k ohm	480	
limitation	22.1k ohm	2171	Applied Now



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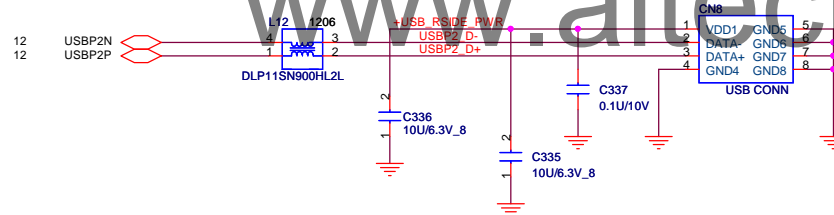
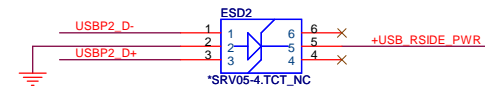


## UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



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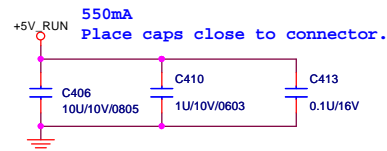
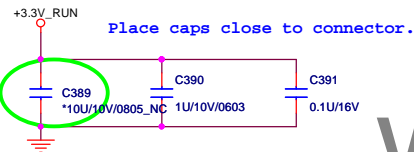
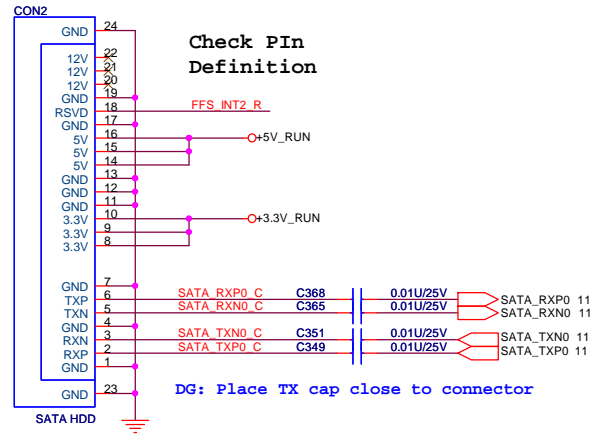
Size	Document Number	Rev
	<b>USB 2.0</b>	1A
Date:	Wednesday, January 19, 2011	Sheet 29 of 61



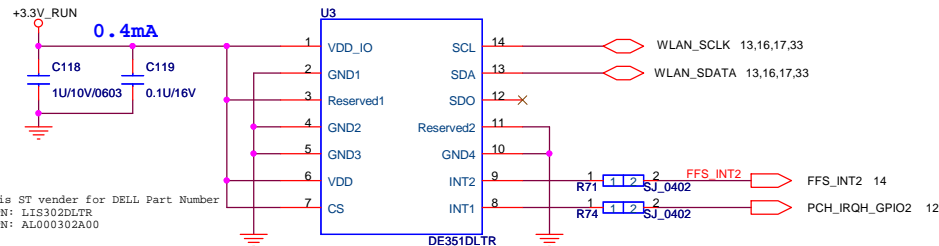




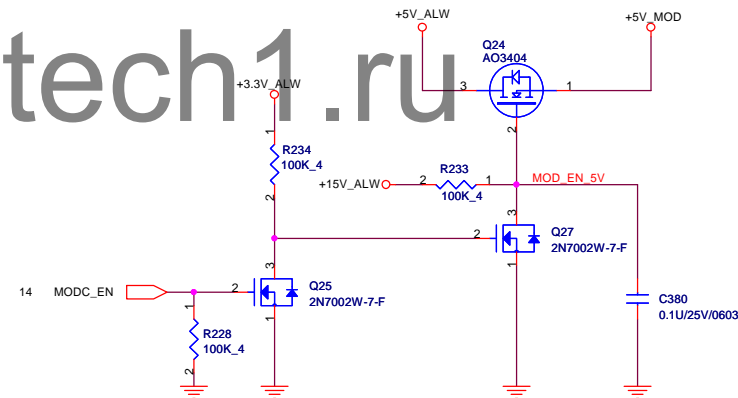
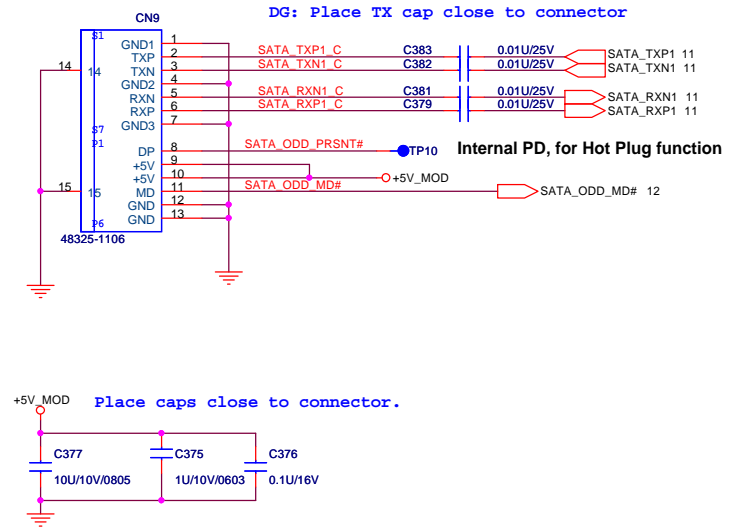
## SATA Connector UM8



## 3-axis Fall Sensor (HDD data protector)



## ODD Connector



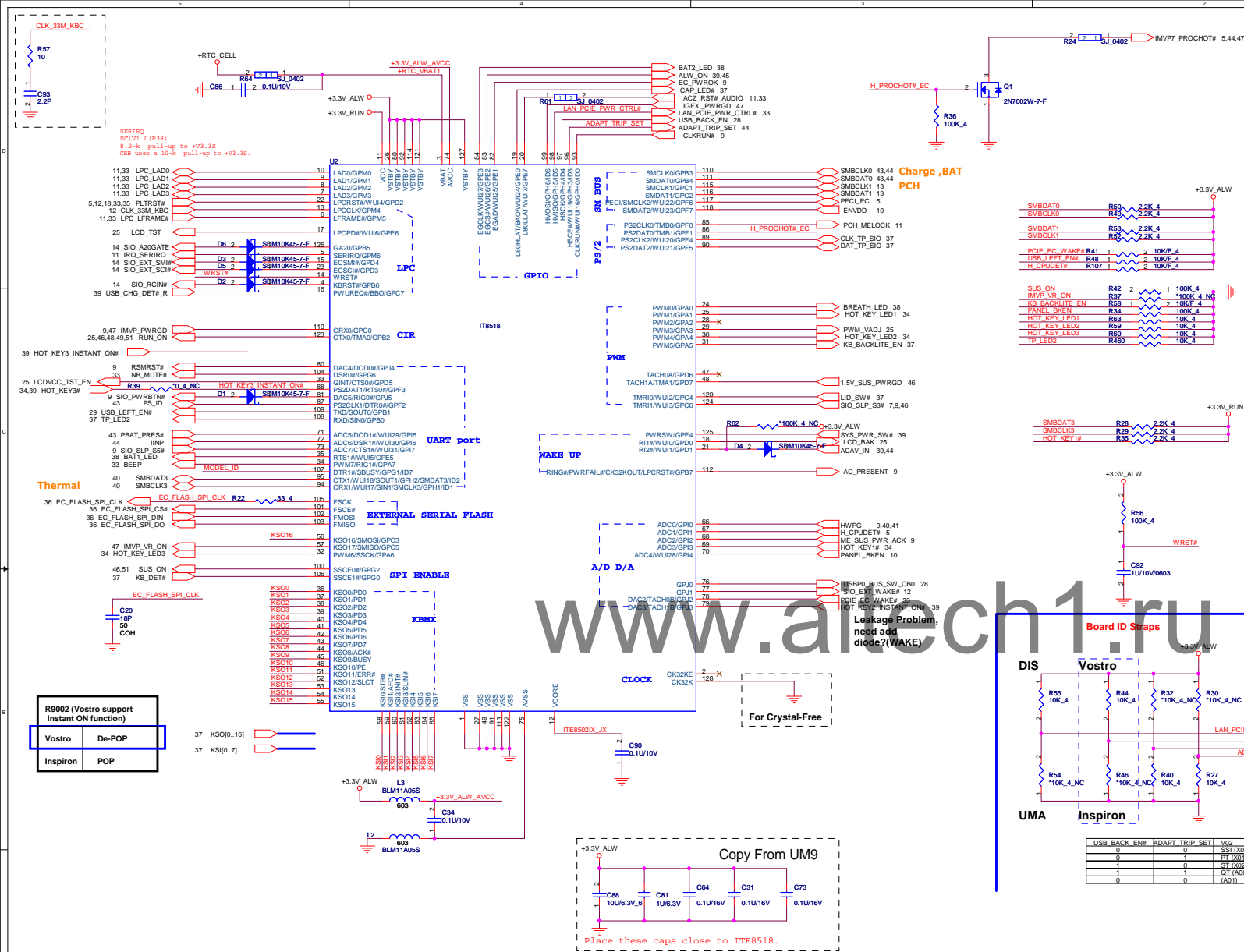
3-axis Fall Sensor	VOSTOR	Inspiron
U3,Q29,D11 R71,R74,R252 C118,C119	POP	NC



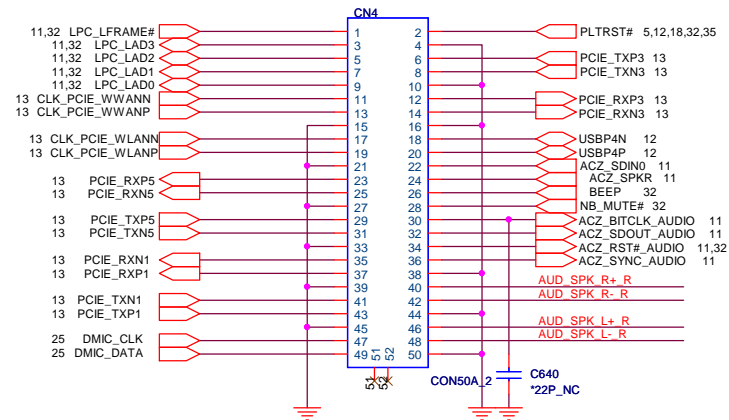
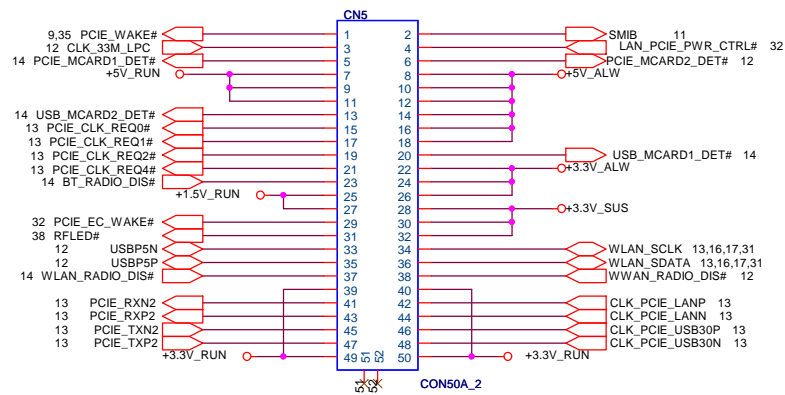
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PROJECT : V02A/RO1A

Size	Document Number	Rev
	<b>SATA HDD/ODD</b>	1A
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**Int. Stereo Speakers**  
5V / 4 Ohm / 2W



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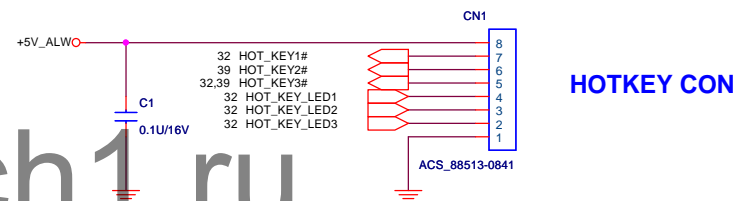
**PROJECT : V02A/R01A**

**SIO (ITE8518E)**

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		1A
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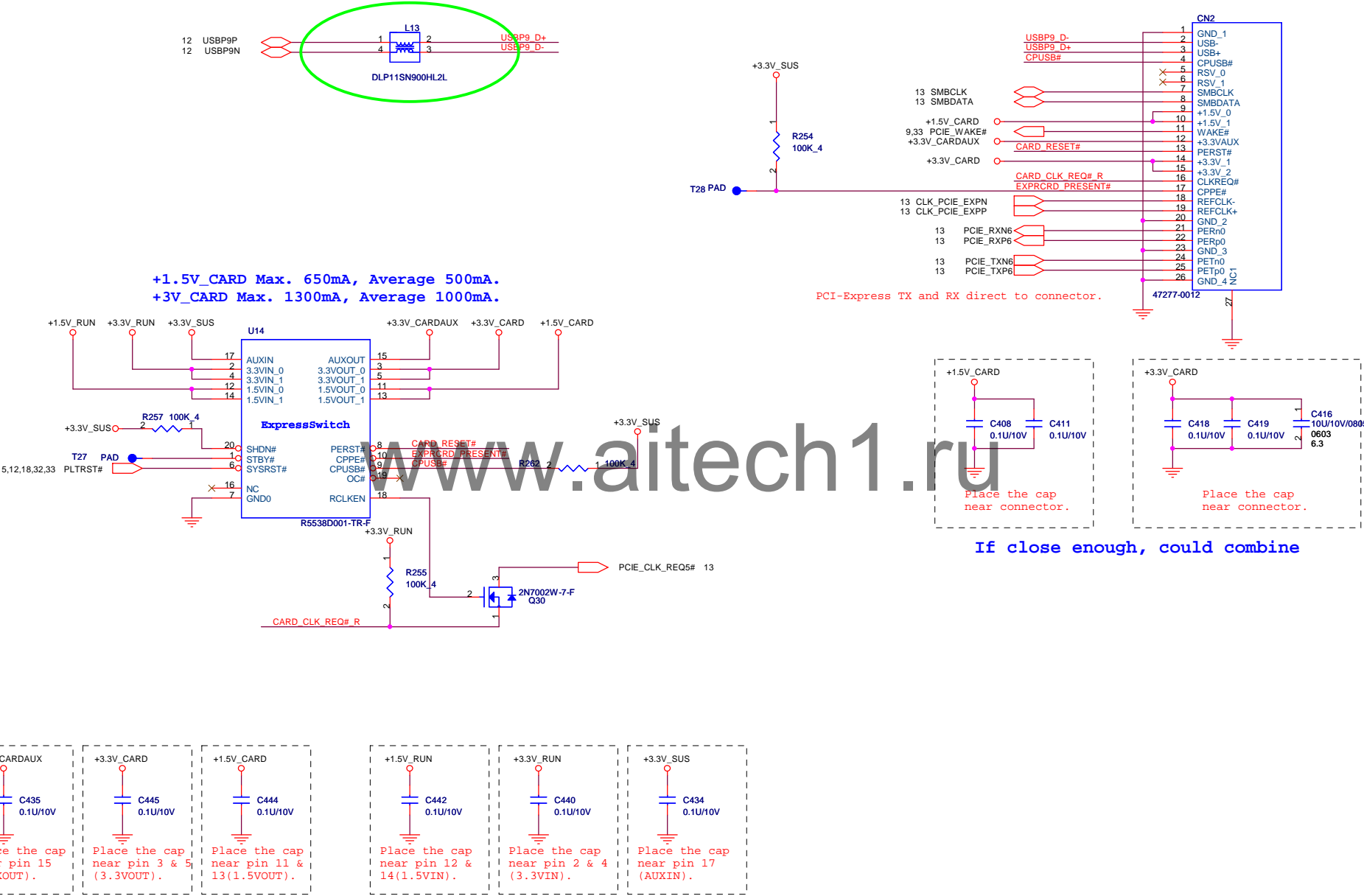
**Quanta Computer Inc.**

**PROJECT : V02A/RO1A**

Size	Document Number	Rev
	<b>MINI-PCI (WLAN/WPAN)</b>	<b>1A</b>
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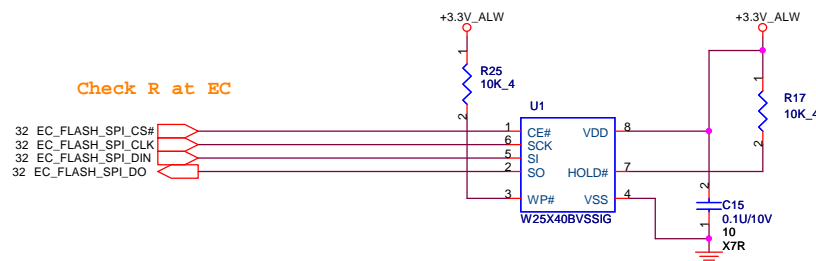


Express Card

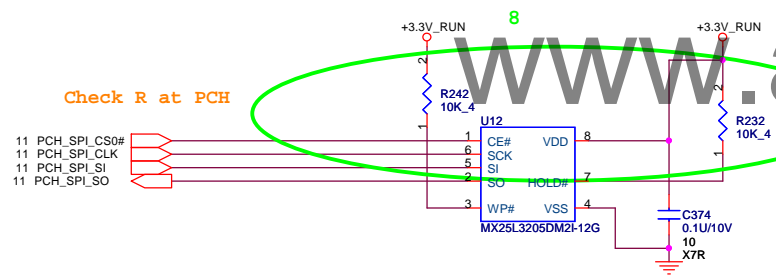




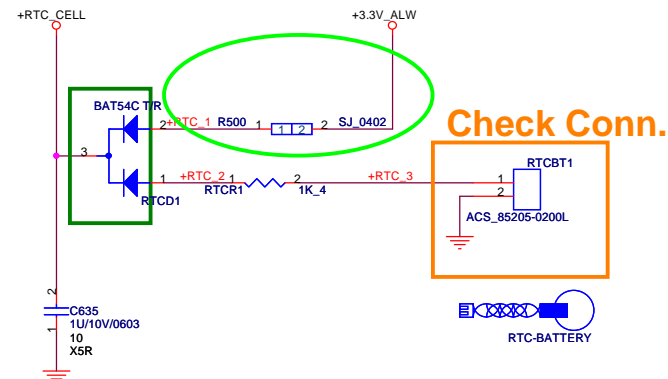
## For EC 4Mbit (512K Byte)



## For PCH 32Mbit (4M Byte)



## RTC



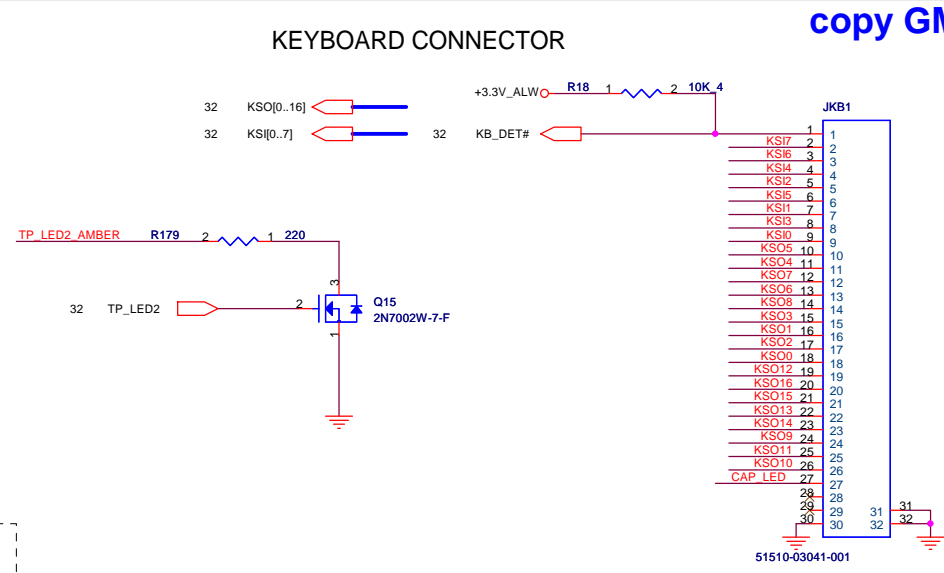
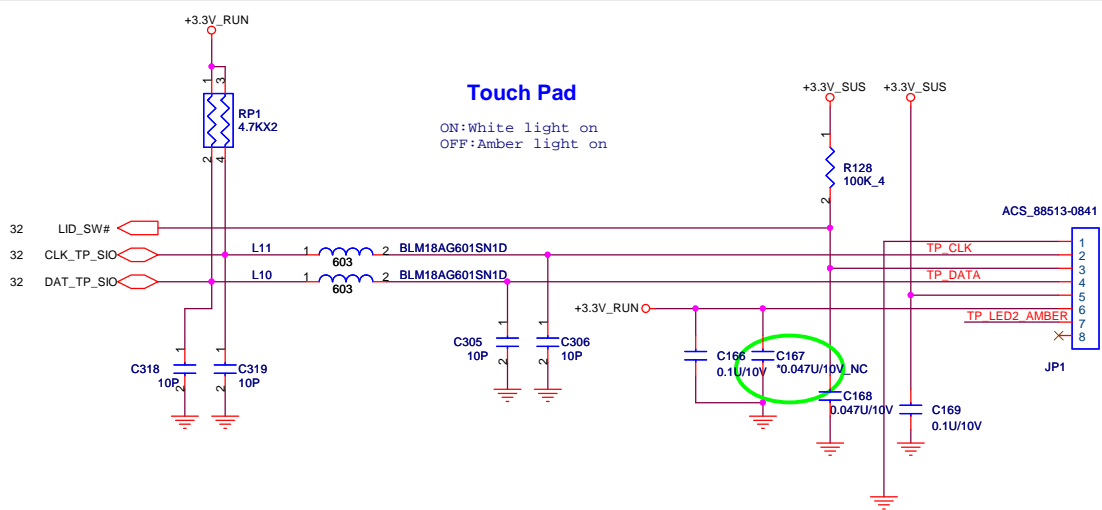
Quanta Computer Inc.

PROJECT : V02A/RO1A

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		1A
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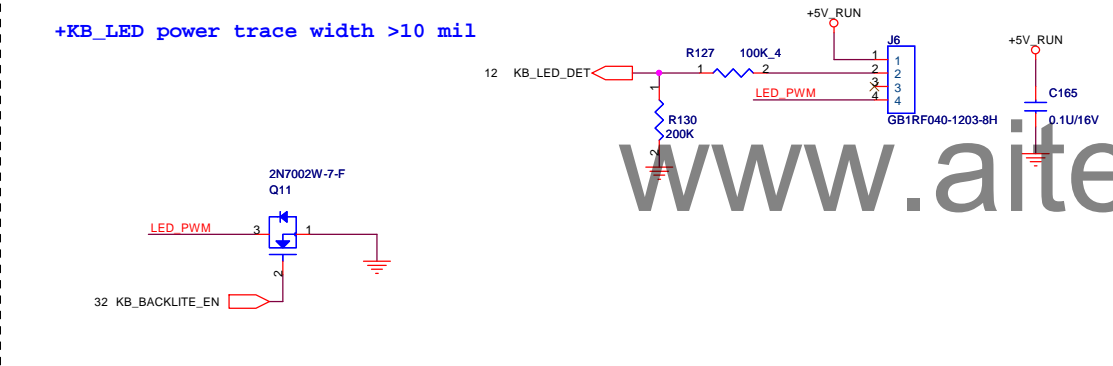
FLASH / RTC





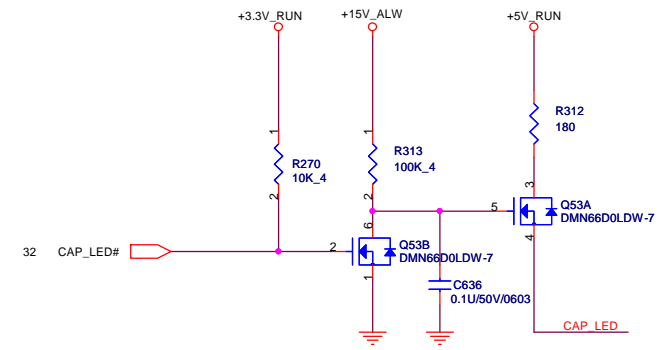
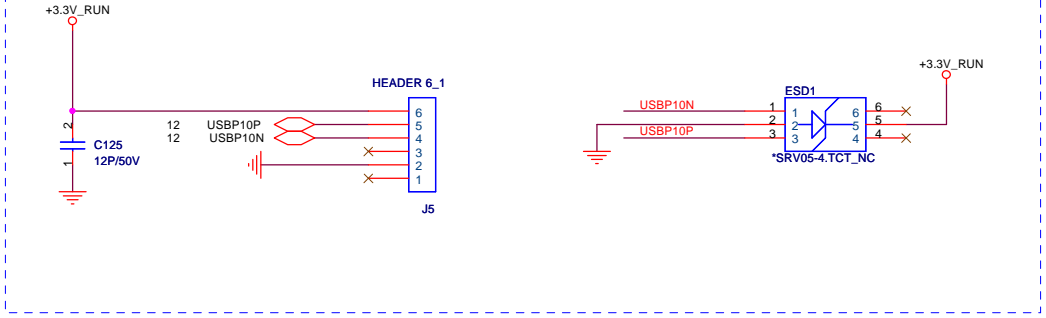
### Key board illumination

+KB\_LED power trace width >10 mil



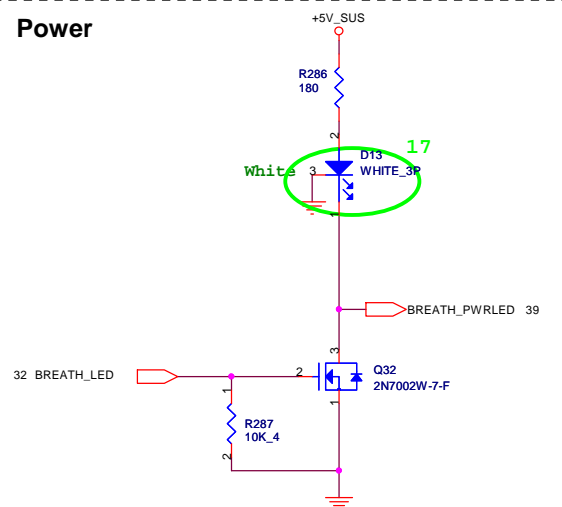
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### Biometric

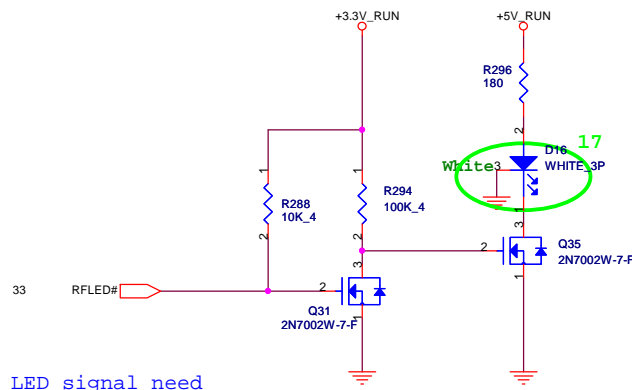




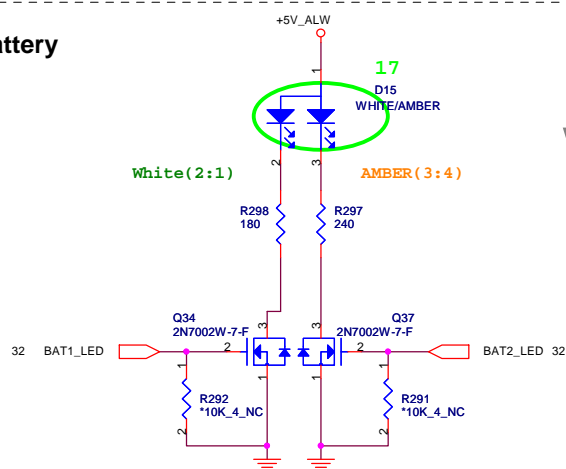
## Power



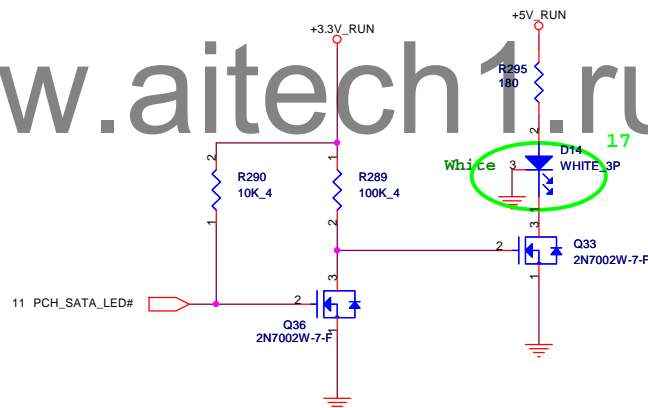
## Bluetooth / WLAN on/off LED



## Battery



## HDD activity LED.



VOSTOR	R286,R295,R296,R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286,R295,R296,R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

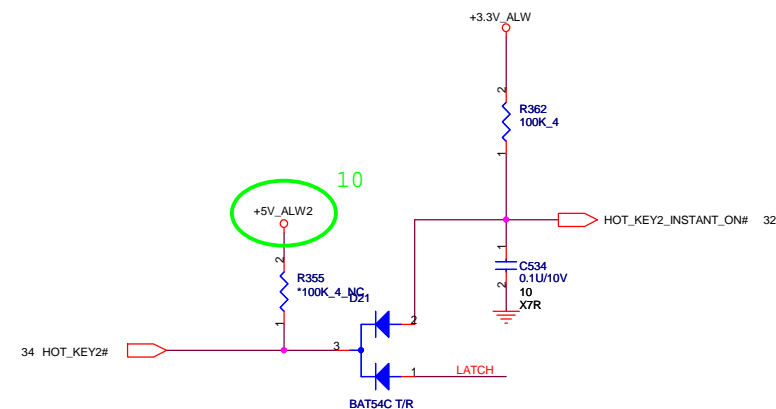
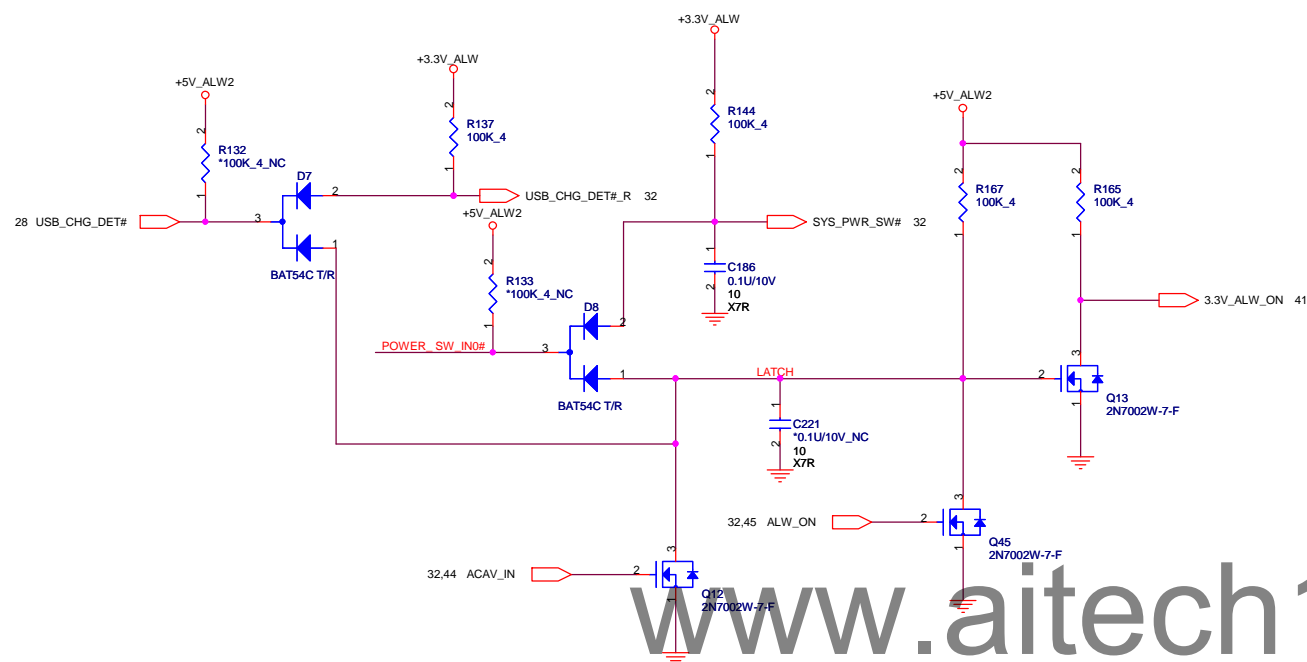


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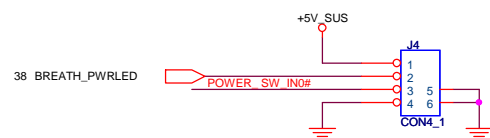


# 3VALW ON POWER LOGIC

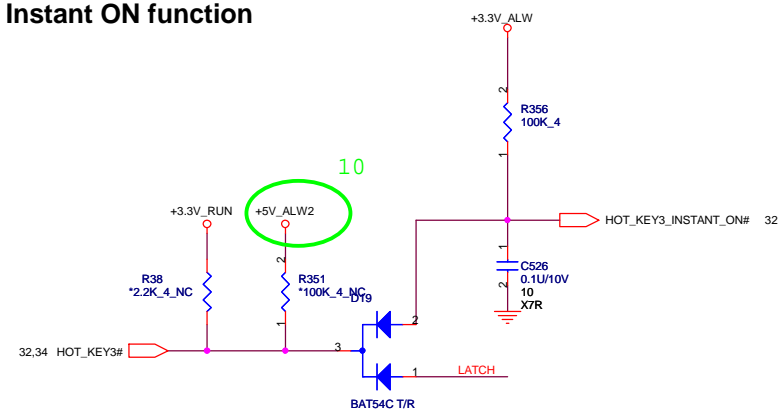


Vostro pop D19,C526,R356 depop R38,R39  
Inspiron depop D19,C526,R356 pop R38,R39

## PWR button board



## Instant ON function



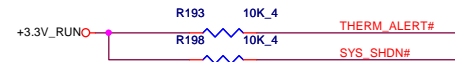
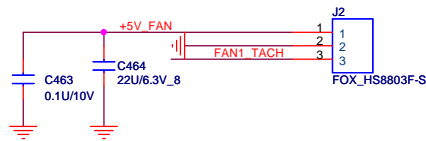
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**PROJECT : V02A/R01A**

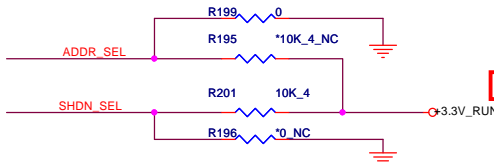
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**PWR SW/LED**

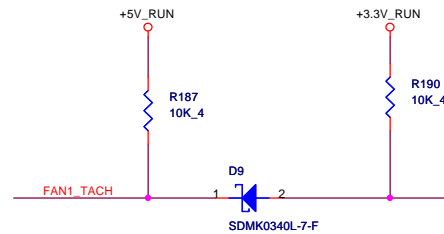




ADDR\_SEL  
HIGH: 0101 110xb  
OPN: 0111 101xb  
GND: 0101 111xb



SHDN\_SEL  
HIGH: External Diode 2 Mode  
OPN: AMD CPU/Diode Mode  
GND: Intel Transistor Mode



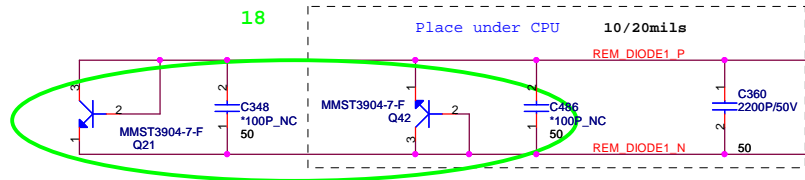
19 VGA\_THERMDN  
C8768 should  
place close to  
GPU

18

Place under CPU

C8767 should  
place close to  
EMC2112

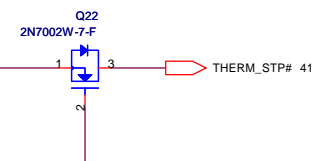
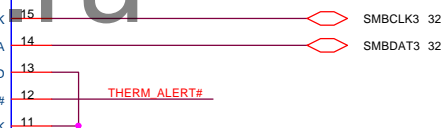
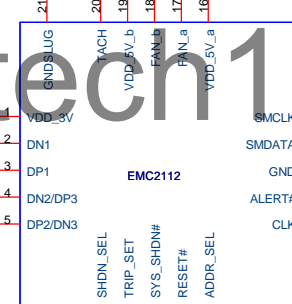
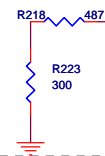
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C314 should  
place close to  
EMC2112

C341  
0.1U/10V

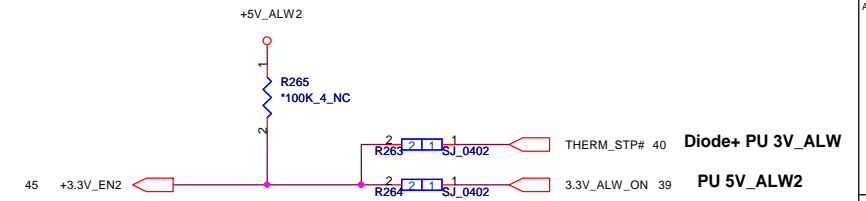
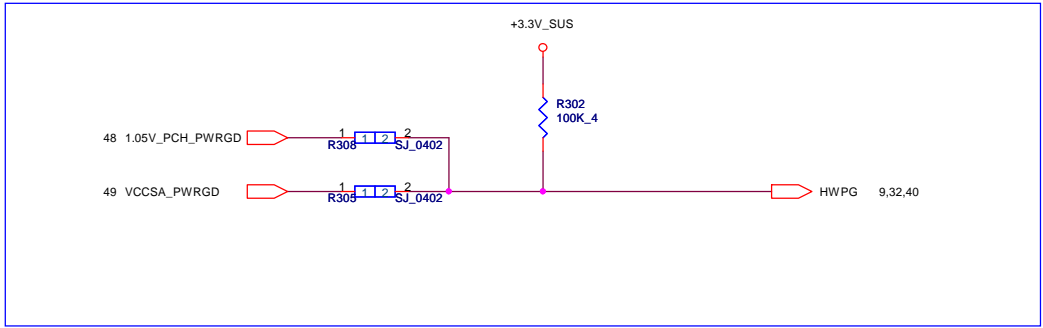
OTP 85 degree C



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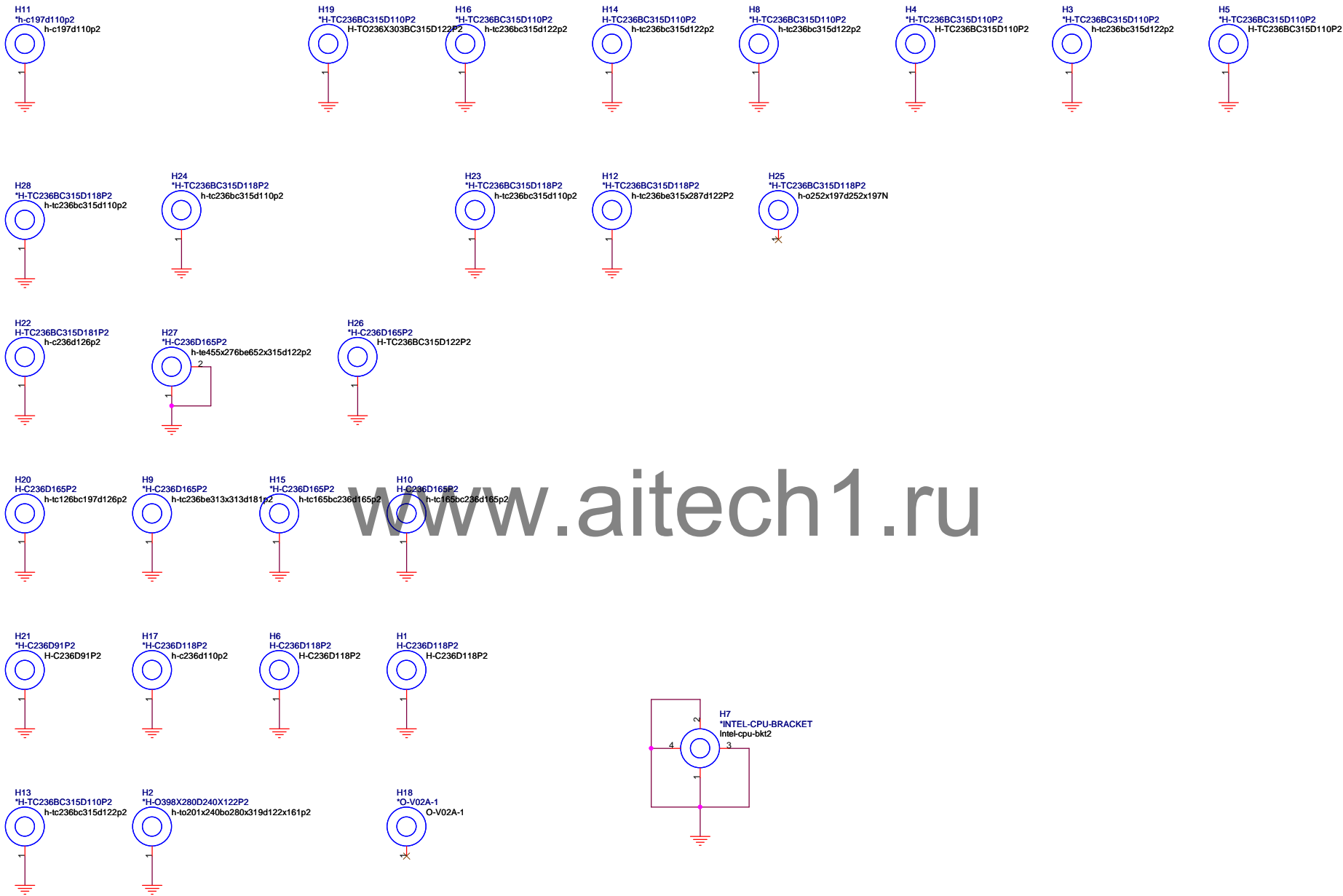
Size	Document Number	Rev
		1A
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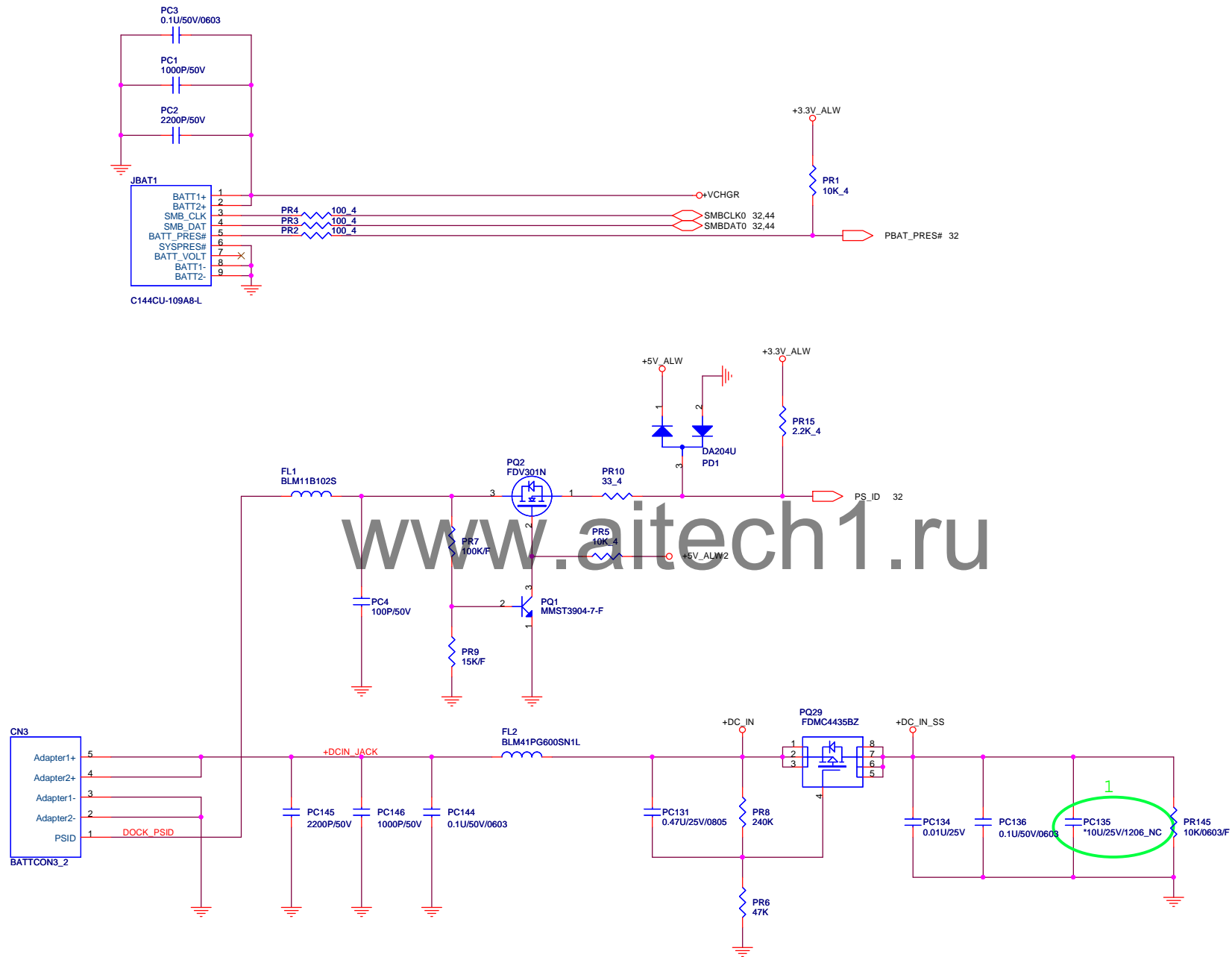


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**PROJECT : V02A/RO1A**

Size	Document Number	Rev
		1A
<b>SCREW PAD</b>		
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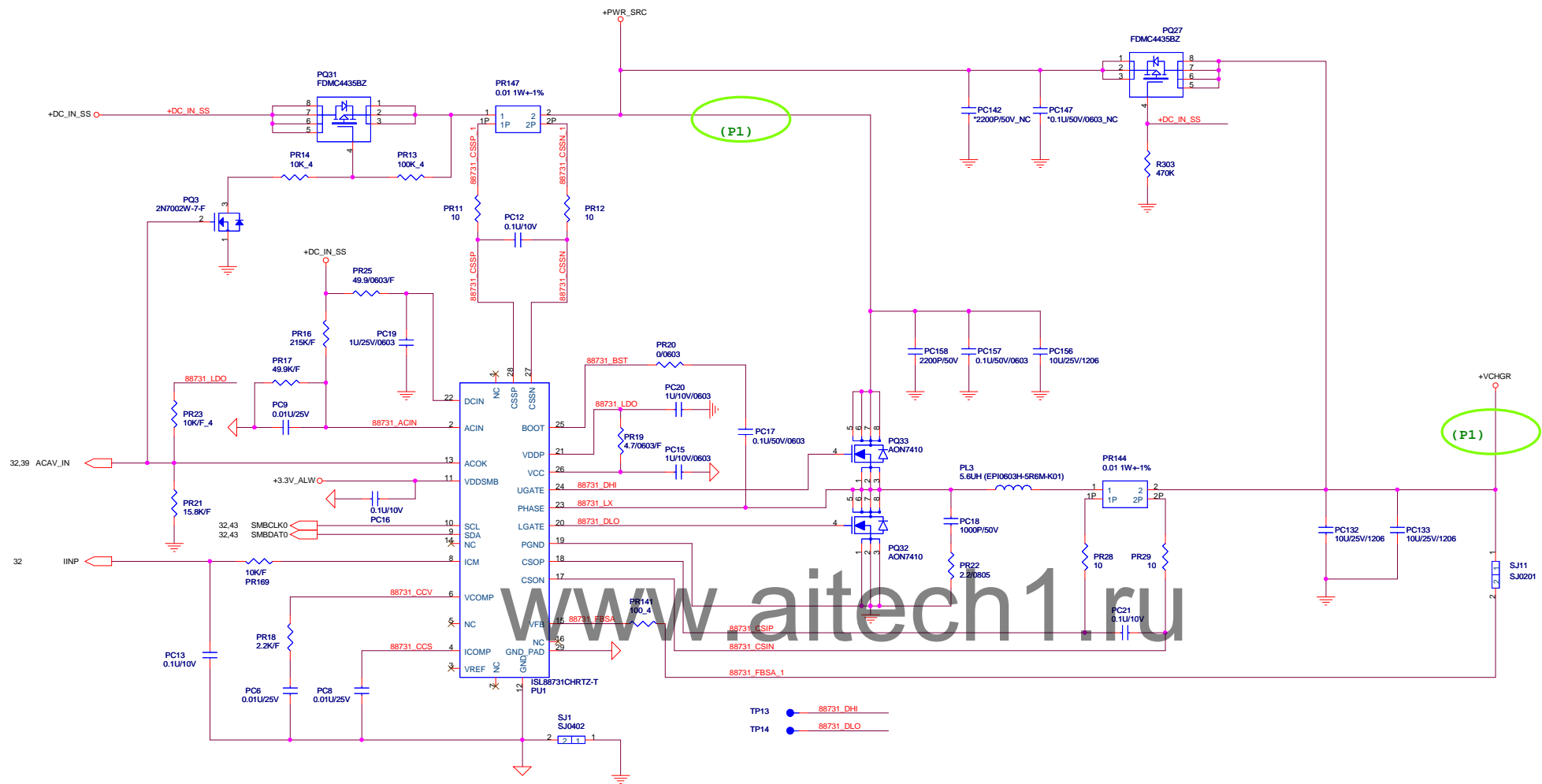


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**PROJECT : V02A/RO1A**

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	<b>DC IN / BATT</b>	1A
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Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A





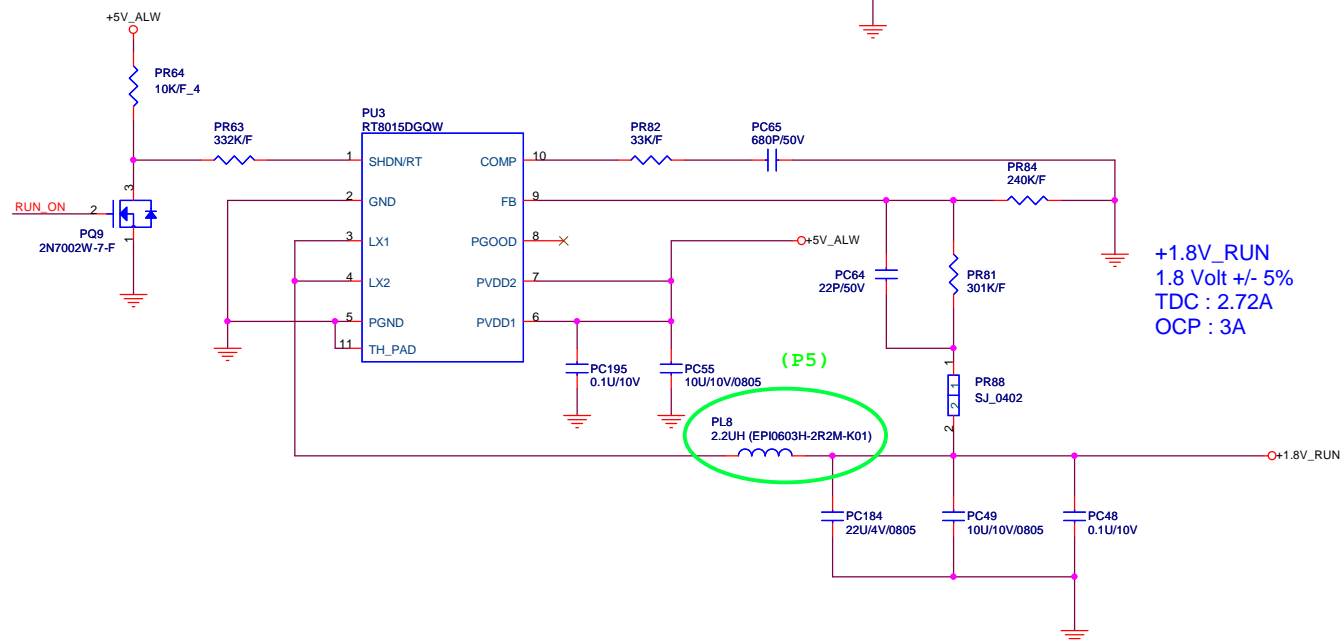
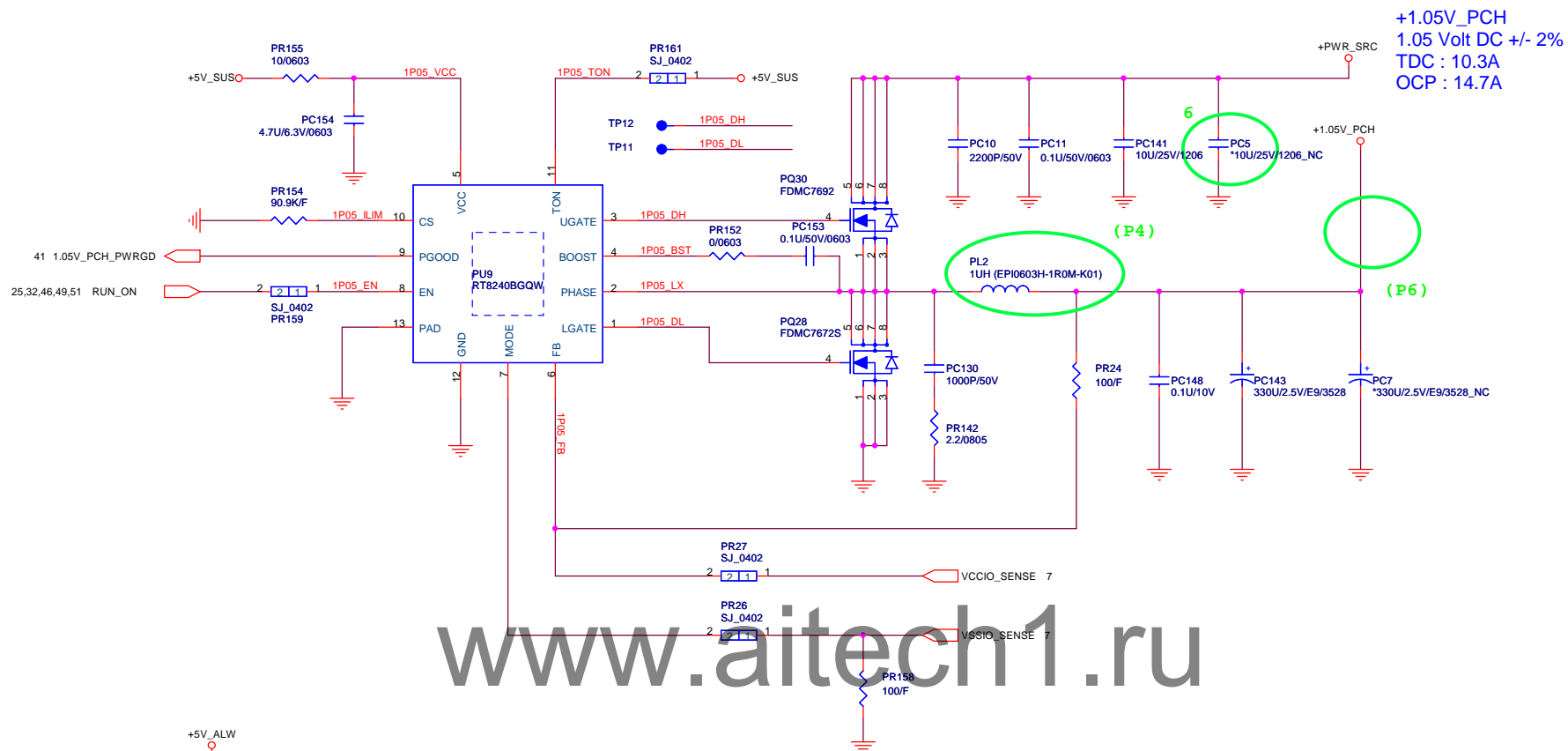








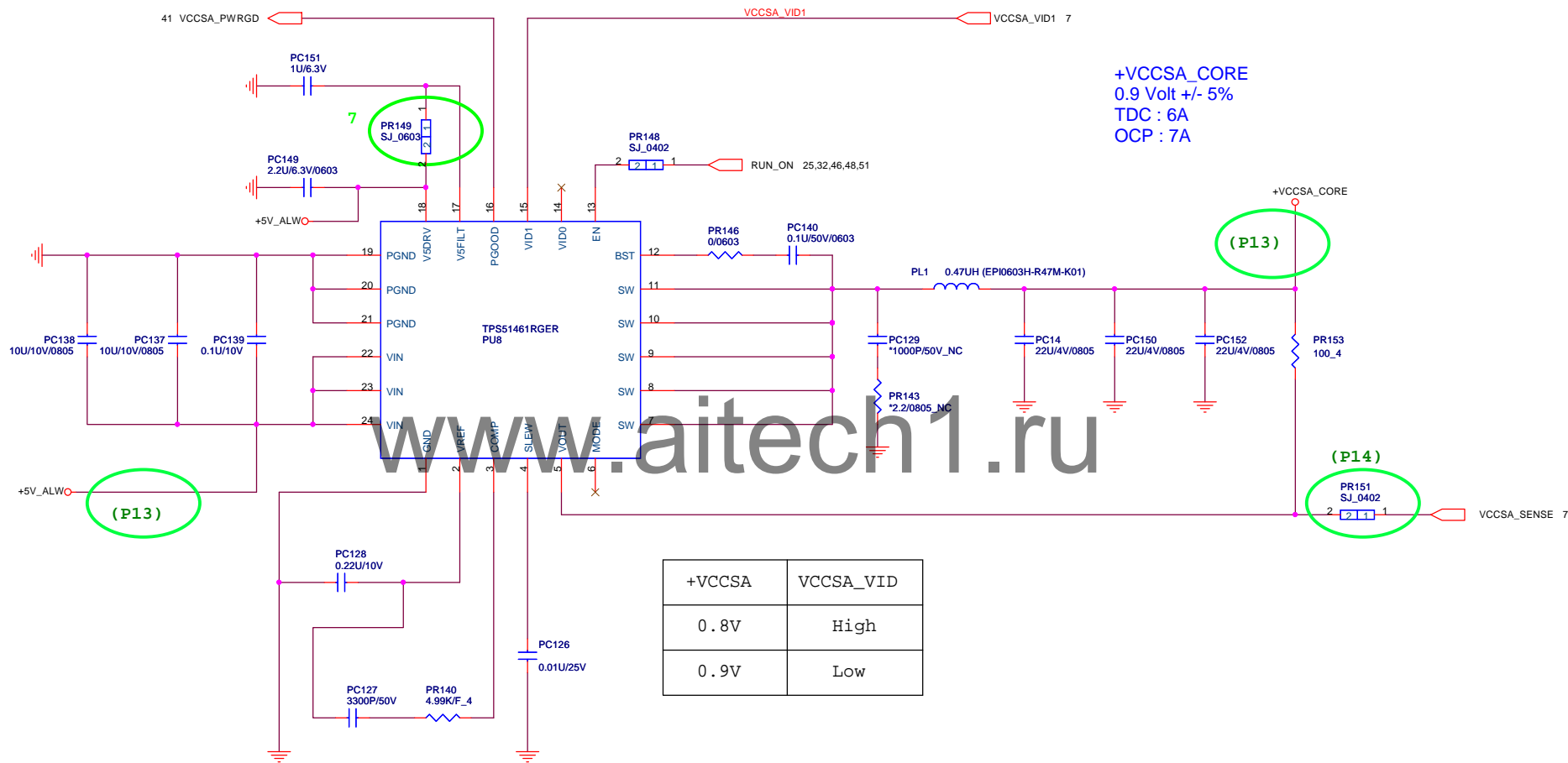




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**PROJECT : V02A/RO1A**

Size	Document Number	Rev
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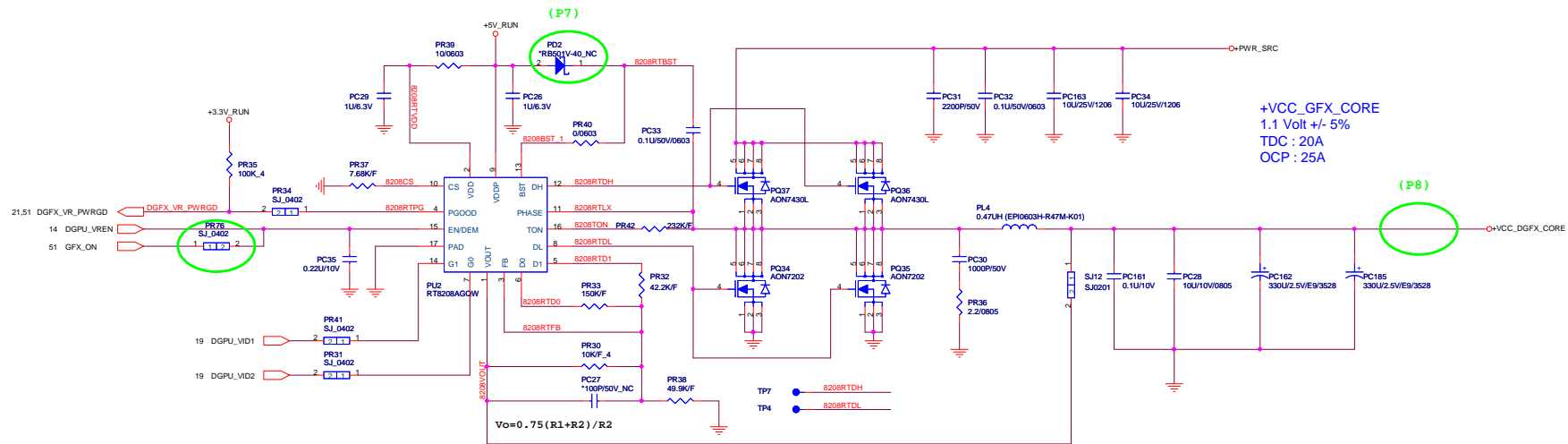




**Quanta Computer Inc.**

**PROJECT : V02A/RO1A**





#### Robson\_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
<b>Setting</b>		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

#### Whistler\_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
<b>Setting</b>		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

#### Seymour\_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
<b>Setting</b>		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K

